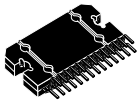
STA510

60V 5A POWER FULL BRIDGE

PRODUCT PREVIEW

- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 150mΩ R_{dsON} NDMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- WARNING OUTPUT: THERMAL, OVERLOAD
- UNDER VOLTAGE PROTECTION ON V_{REG}
- OVERVOLTAGE PROTECTION
- TWO LEVELS CURRENT PROTECTION

MULTIPOWER BCD TECHNOLOGY



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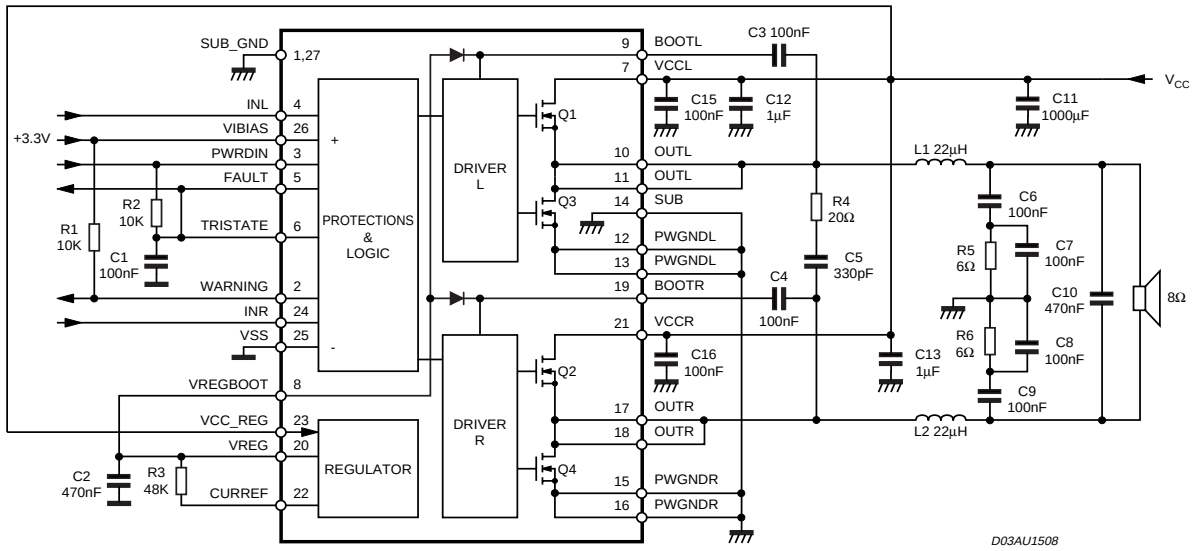
ORDERING NUMBER: STA510

DESCRIPTION

STA510 is a monolithic full bridge stage in Multipower BCD Technology. The device is particularly designed to make the output stage of classD audio amplifier capable to deliver 100W undistorted output power on 8Ω load. The input pins have threshold proportional to V_{Ibias} pin voltage. The commutation speed of the output stage is settable with an extenal resistor (Curref pin) to choice for each application the best compromise of THD versus EMI and current spikes.

The overcurrent protection works in two steps, the first one, at a lower value limits the current terminating the pulse (independently to the input) when the current in the power output MOS reaches a first threshold: it is aimed to act in case of overload and its effect is to stabilize the mean current in the load to a limit value. The second step shuts down completely the device and restarts the power on sequence if the current reaches a second (higher) threshold: it is aimed to act in case of short circuit, when the first limitation can fail.

AUDIO APPLICATION CIRCUIT



PIN FUNCTION

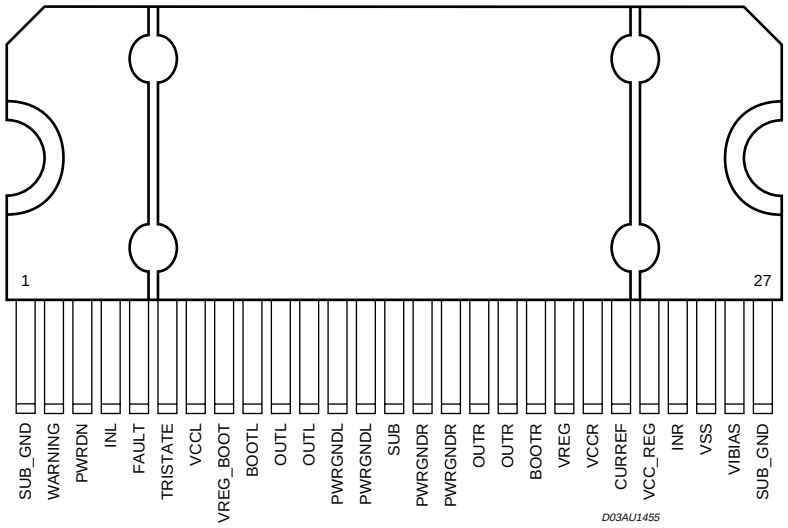
N°	Pin	Description
1, 27	SUB_GND	Substrate (frame) and signal ground
2	WARNING	Warning advisor
3	PWRDN	St-by input pin
4	INL	Input left arm
5	FAULT	Fault adviosor
6	TRISTATE	Hi-Z input pin
7	VCCL	Positive power supply left arm
8	VREG_BOOT	VREG input for bootstrap charging
9	BOOTL	Bootstrap cap. left arm
10, 11	OUTL	Output left arm
12,13	PWRGNDL	Power GND left arm
14	SUB	Substrate (plug near powers)
15, 16	PWRGNDR	Power GND right arm
17, 18	OUTR	Output right arm
19	BOOTR	Bootstrap cap. right arm
20	VREG	Regulator output (for filtering)
21	VCCR	Positive power supply right arm
22	CURREF	Resistor for commutation speed setting
23	VCC_REG	Positive power supply for the regulator
24	INR	Input right arm
25	VSS	Input logic ground
26	VIBIAS	High logic state setting voltage

FUNCTIONAL PIN STATUS

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT*	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorpion
PWRDN	1	Normal operation
WARNING	0	Temperature of the IC =130°C; overload
WARNING*	1	Normal operation

* : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CE}	DC Supply Voltage (VCCR, VCCL, VCC_REG)	60	V
V_{max}	Logic Voltage (INL, INR, VIBIAS, TRISTATE, PWRDN)	5.5*	V
V_{REG}	Regulator Voltage (VREG, VREG_BOOT, CURREF)	8	V
v_{od}	Voltage on Open Drain Pins (WARNING, FAULT)	60	V
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

*: referred to V_{SS}

ELECTRICAL CHARACTERISTCS (V_{Ibias} = 3.3V; Vcc = 45V; T_{amb} = 25°C unless otherwise specified referred to “AUDIO APPLICATION CIRCUIT” pag. 1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Nchannel MOSFET RdsON	Id=1A;		0.15	0.20	Ω
I_{dss}	Power Nchannel leakage Idss			TBD		µA
G_{NH}	Power Nchannel RdsON Matching	Id = 1A; High Right with High Left	95			%
G_{NL}	Power Nchannel RdsON Matching	Id = 1A; Low Right with Low Left	95			%
D_{t-s}	Low current Dead Time (static)	see test circuit in fig. 1		20	40	ns
D_{t-d}	High current Dead Time (dinamic)	Id = 5A; see fig 3		40	80	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load;			100	ns

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time	Resistive load;			50	ns
t_f	Fall time	Resistive load;			50	ns
V_{CC}	Supply voltage operating range		11		55	V
V_{IN-H}	High level input voltage			$V_{Ibias}/2$ +150mV	$V_{Ibias}/2$ +300mV	V
V_{IN-L}	Low level input voltage		$V_{Ibias}/2$ -300mV	$V_{Ibias}/2$ -130mV		V
I_{IN-H}	Hi level Input current	Pin voltage = V_{Ibias}			1	µA
I_{IN-L}	Low level input current	Pin voltage = 0.3V			1	µA
$I_{PWRDN-H}$	Hi level PWRDN pin input current	Ibias = 3.3V		35		µA
V_L	Low logical state voltage (pin PWRDN, TRISTATE)	Ibias = 3.3V	0.8	1		V
V_H	High logical state voltage (pin PWRDN, TRISTATE)	Ibias = 3.3V		1.9	2.2	V
$I_{VCC-PWRDN}$	Supply current from Vcc in Power Down	PWRDN = 0; TRISTATE = 0		0.25		mA
$I_{VCC-hiz}$	Supply current from Vcc in Tri-state	PWRDN = 1; Tri-state=0;		TBD		mA
I_{VCC}	Supply current from Vcc in operation	No LOAD Input pulse width = 50% Duty; Switching Frequency = 384Khz; No LC filters;		100		mA
I_{lim}	Current Limit (Overload)		6	7	8	A
I_{sc}	Short circuit current threshold		7	8	9	A
V_{UV}	Undervoltage protection threshold on VREG			7		V
V_{OV}	Overvoltage protection threshold on VCC		55	60		V
V_{DROP}	Dropout from VCC to VREG			4		V

LOGIC TRUTH TABLE (see fig. 2)

TRI-STATE	INL	INR	HSL (Q1)	HSR (Q2)	LSL (Q3)	LSR (Q4)	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 1. Test Circuit.

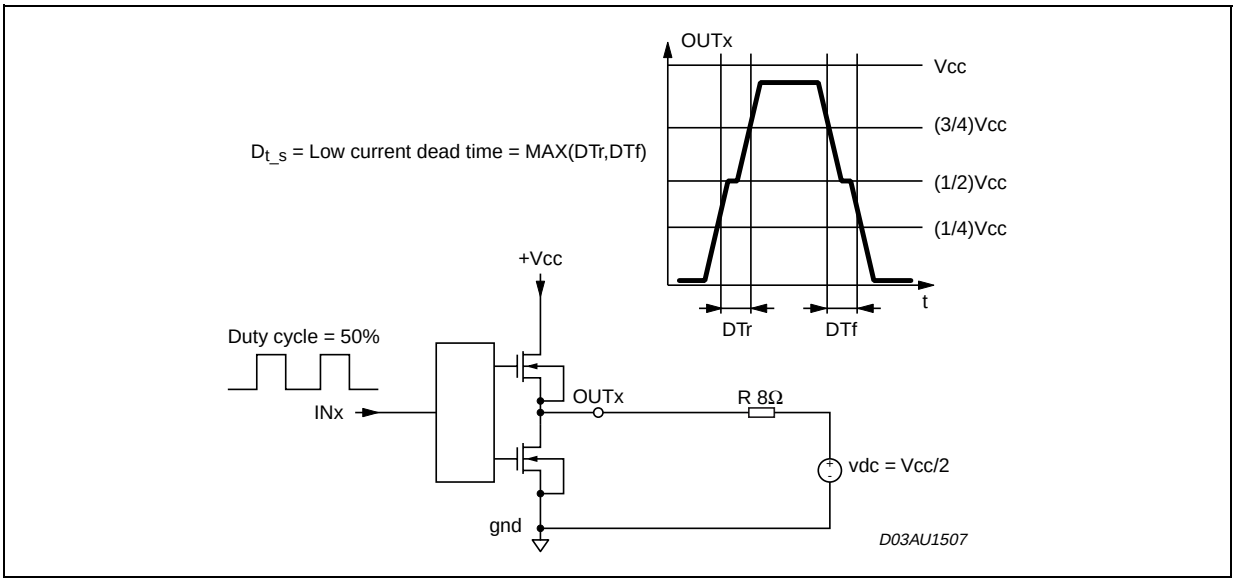


Figure 2.

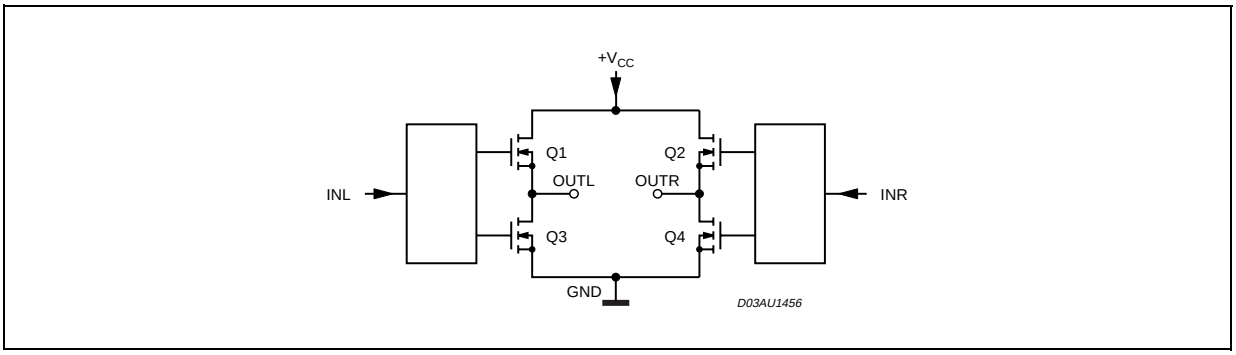
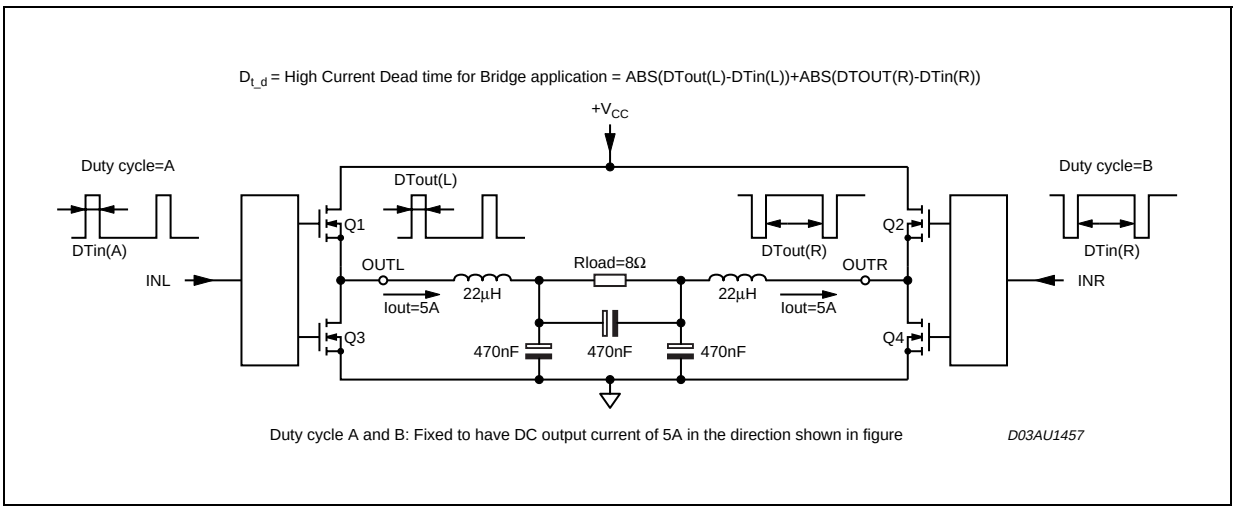


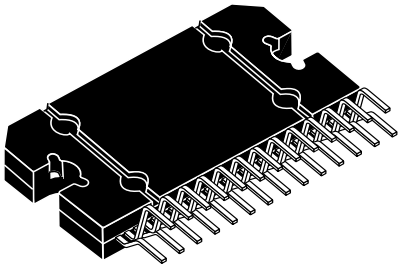
Figure 3.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



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