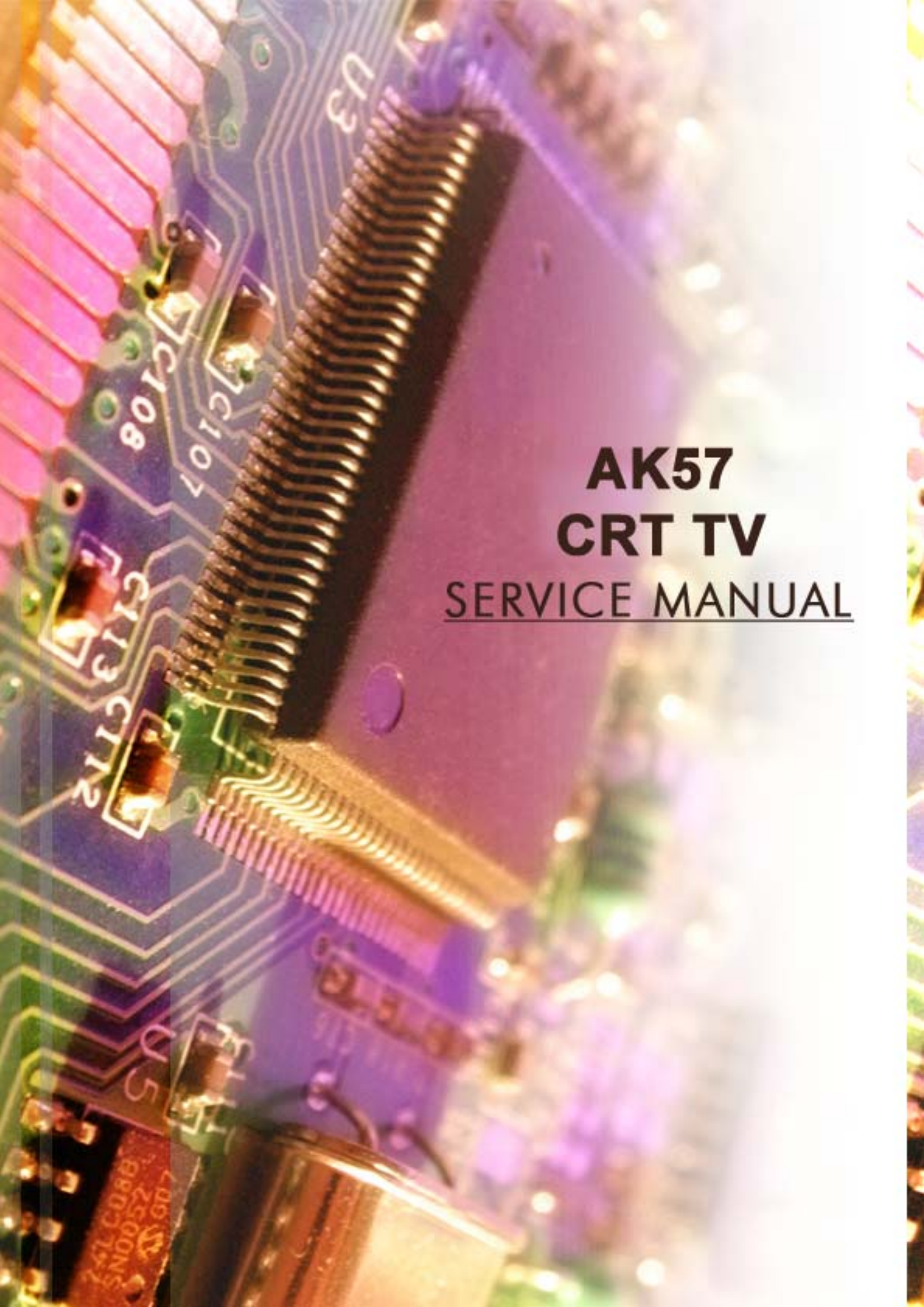


AK57
CRT TV
SERVICE MANUAL

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1. Introduction

1.1. Purpose

This document is prepared for the UOCII TV project and describes the whole system features and operating principles to be used in hardware design phase.

The document is based on "Device Specification UOCII-Version 1.12" from **Philips Semiconductors**.

Prior to hardware design start, all parties involved must agree with the contents of this document.

1.2. Scope

The document covers detailed descriptions of 11AK56 chassis system building blocks.

1.3. General Features

11AK57 is a 90° / 50 Hz. chassis which is capable of driving 14" superflat and 15" realflat CRT's .

The chassis will have the following main features;

- Remote Control
- 100 programs
- On Screen Display
- Mono
- Colour Standarts ; PAL, SECAM, NTSC,
- Transmission standarts ; B/G, L/L' I/I', DK,
- Teletext ; One pages,
- Multi-standard alignment free PLL tuning,
- DVD or DVIX Player
- DVB-T option
- Europe Scart
- Detachable headphone output option,
- Front or side or back AV input option,
- Back AV output option,
- Coaxial output for IDTV/DVB-T
- 2W (%10 THD),
- 90-270V 50Hz or 170V-270V 50Hz SMPS
- Less than 3W
- DVD-Video, DVD R/RW, CD-R/RW, CD-Audio and MP3 Audio, JPEG (Picture CD), Video CD and its sub formats like CVD, SVCD, DVCD.

2. General Description

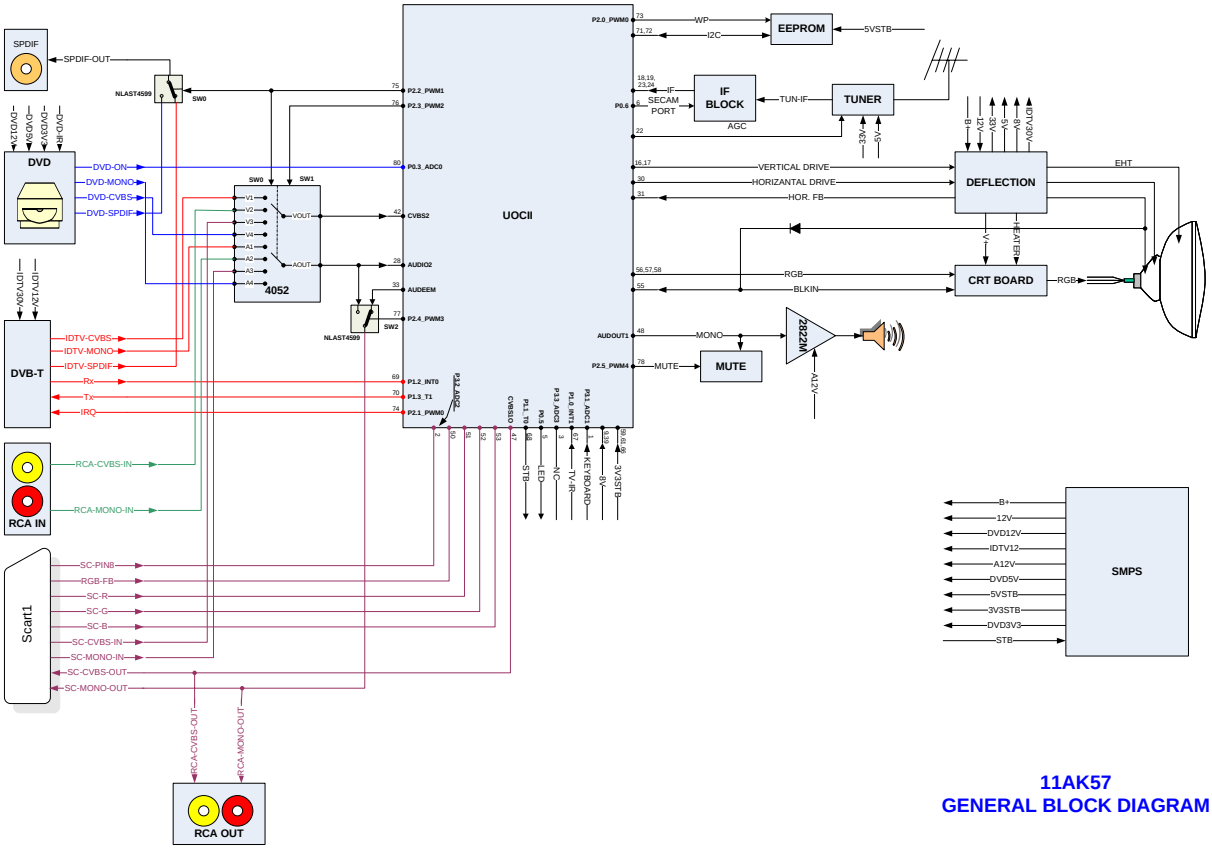
2.1. Introduction

This chapter describes system building blocks and their detailed descriptions.

2.2. System Building Blocks

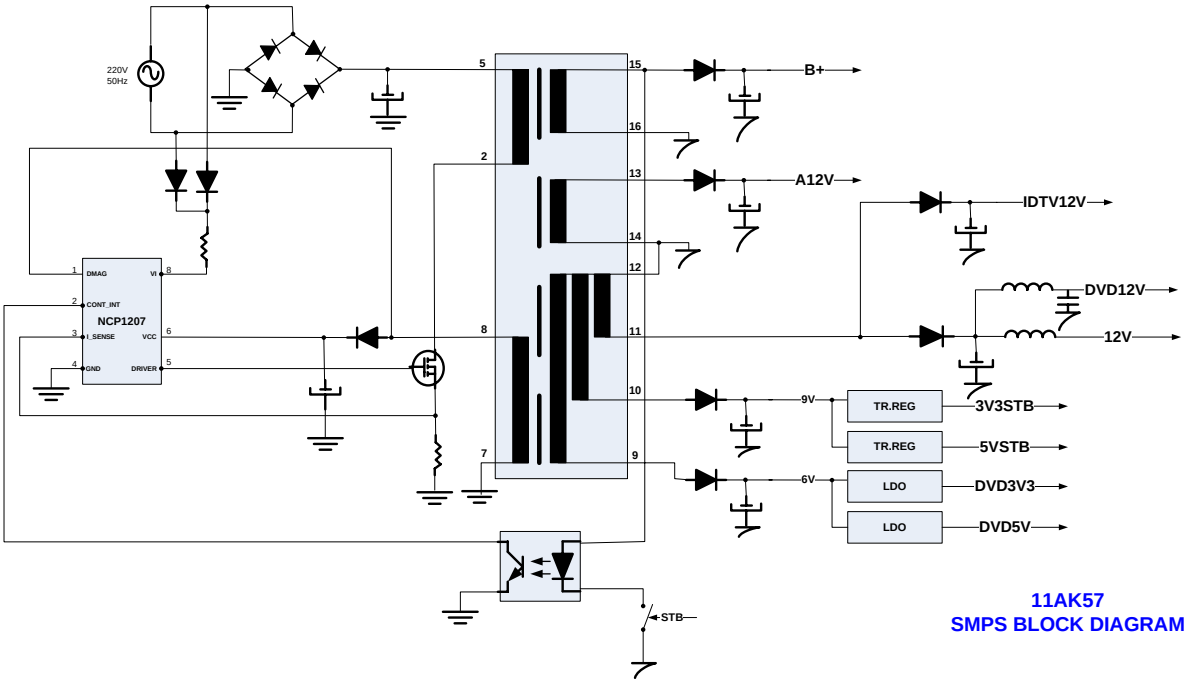
2.2.1. AK57 Chassis Block Diagrams

2.2.1.1. Genaral



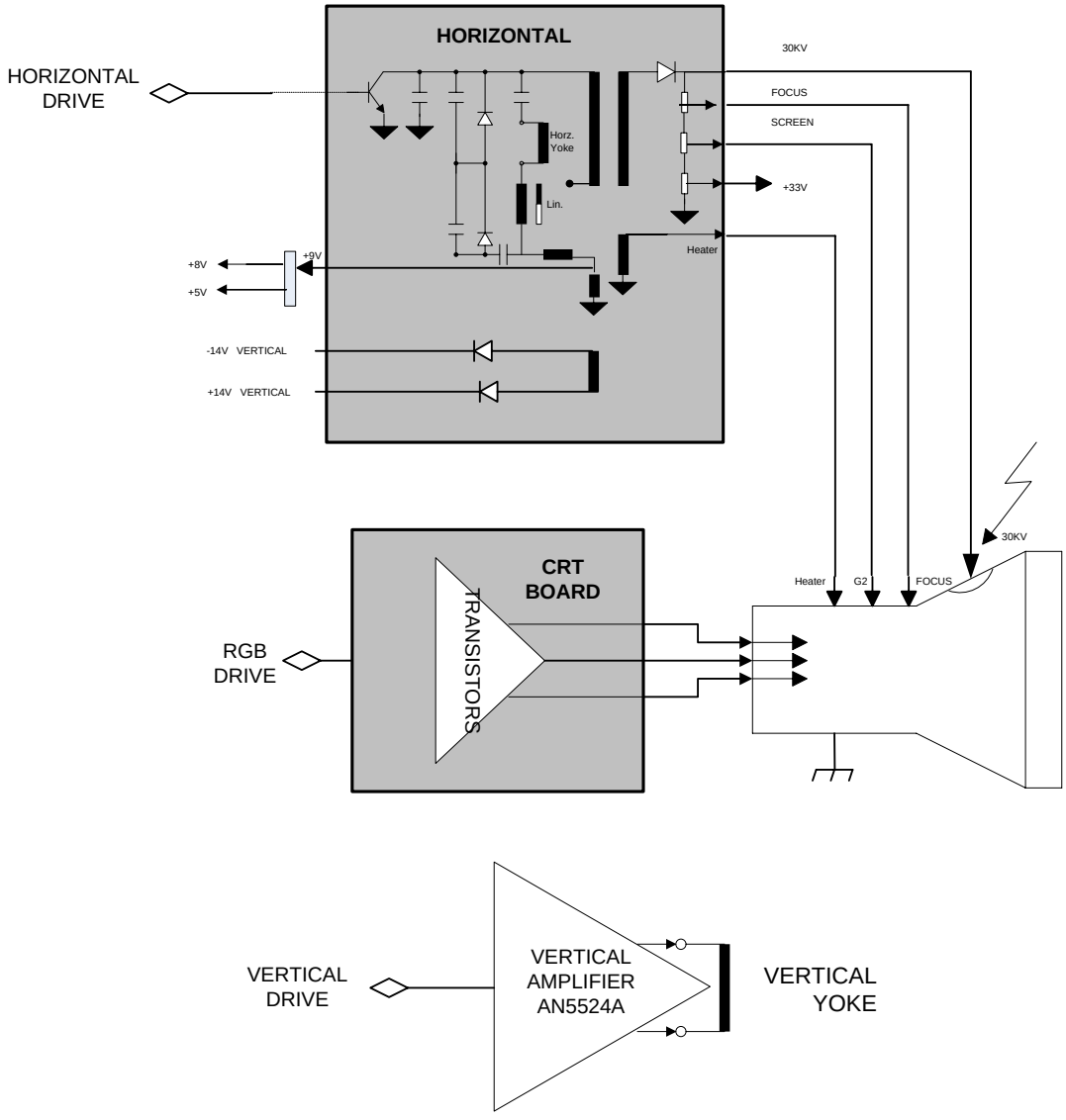
11AK57
GENERAL BLOCK DIAGRAM

2.2.1.2. SMPS



11AK57
SMPS BLOCK DIAGRAM

2.2.1.3. DEFLECTION



2.2.2. AK57 Chassis Main Blocks

AK57 chassis main blocks are;

- **UOCII** : Microcontroller + Video Proccessor + Sound Proccessor + IF + Teletext
- **AUDIO** : Audio Amp.,
- **EXT. AV I/O** : Scart , AV input, AV output,
- **AV SWITCHING** : 4052, 4599
- **TUNER** : PLL Tuner

- **SAW FILTERS**
- **SMPS** : SMPS Controller, SMT, Bridge Rect., Line Filters
- **DEFLECTION** : FBT, HOT, Vertical Amplifier, Line Driver,
- **CRT BOARD** : RGB Amp. with transistors,

2.2.2.1. UOC-II (ULTIMATE-ONE-CHIP)

UOCII is composed of microcontroller, video proccessor, sound proccessor and IF blocks.

The various versions of the TDA955X H/N1 series combine the functions of a video processor together with a microcontroller.The ICs are intended to be used in economy television receivers with 90 and 110 degree picture tubes.

The ICs have supply voltages of 8V and 3.3V and they are mounted in a QFP 80 envelope.

The features are given in the following feature list.

FEATURES

TV-signal processor

- Multi-standard vision IF circuit with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- The QSS and mono FM functionality are both available so that an FM/AM TV receiver can be built without the use of additional ICs
- The mono intercarrier sound circuit has a selective
- FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- The FM-PLL demodulator can be set to centre frequencies of 4.74/5.74 MHz so that a second sound channel can be demodulated. In such an application it is necessary that an external bandpass filter is inserted.
- The vision IF and mono intercarrier sound circuit can be used for the demodulation of FM radio signals
- Video switch with 2 external CVBS inputs and a CVBS output. One of the CVBS inputs can be used as Y/C input.
- 2 external audio inputs. The selection of the various inputs is coupled to the selection of the CVBS signals
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Switchable group delay correction in the CVBS path
- Picture improvement features with peaking (with switchable centre frequency, depeaking, variable positive/negative overshoot ratio and video dependent coring), dynamic skin tone control and blue-, black- and white stretching
- Integrated chroma band-pass filter with switchable centre frequency
- Switchable DC transfer ratio for the luminance signal
- Only one reference (12 MHz) crystal required for the m-Controller, Teletext- and the colour decoder
- PAL/NTSC or multi-standard colour decoder with automatic search system

- Internal base-band delay line
- Indication of the Signal-to-Noise ratio of the incoming CVBS signal
- A linear RGB/YUV/YPBPR input with fast blanking for external RGB/YUV sources. The synchronisation circuit can be connected to the incoming Y signal. The Text/OSD signals are internally supplied from the
- m-Controller/Teletext decoder.
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off-set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- Contrast reduction possibility during mixed-mode of OSD and Text signals
- Adjustable 'wide blanking' of the RGB outputs
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes
- Low-power start-up of the horizontal drive circuit

Microcontroller

- 80C51 m-controller core standard instruction set and timing
- 1 ms machine cycle
- 32 - 128Kx8-bit late programmed ROM
- 3 - 12Kx8-bit DataRAM (shared between Display, Acquisition and Auxiliary RAM)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- One 16-bit Timer with 8-bit Pre-scaler
- WatchDog timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- Stand-by, Idle and Power Down modes
- 14 bits PWM for Voltage Synthesis Tuning
- 8-bit A/D converter with 4 multiplexed inputs
- 5 PWM (6-bits) outputs for control of TV analogue signals
- 18 general I/O ports

Data Capture

- Text memory for 1 or 10 pages
- In the 10 page versions inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Data Capture for US Closed Caption
- Data Capture for 525/625 line WST, VPS (PDC system A) and Wide Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimized m-processor throughput

- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for video and WST/VPS data types
- Comprehensive teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

Display

- Teletext and Enhanced OSD modes
- Features of level 1.5 WST and US Close Caption
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 4096 colour palette
- Globally selectable scan lines per row (9/10/13/16) and character matrix [12x10, 12x13, 12x16 (VxH)]
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen display characters
- 4 WST Character sets (G0/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device

Optional Used ICs at AK57 chassis are TDA9550 H/N1, TDA9551 H/N1, TDA9552 H/N1.

FUNCTIONALOF TDA9550 H/N1

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch
- Automatic Volume Levelling
- PAL decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext
- Close Captioning

FUNCTIONALOF TDA9551H

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch

- Automatic Volume Levelling
- PAL decoder
- SECAM decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext
- Close Captioning

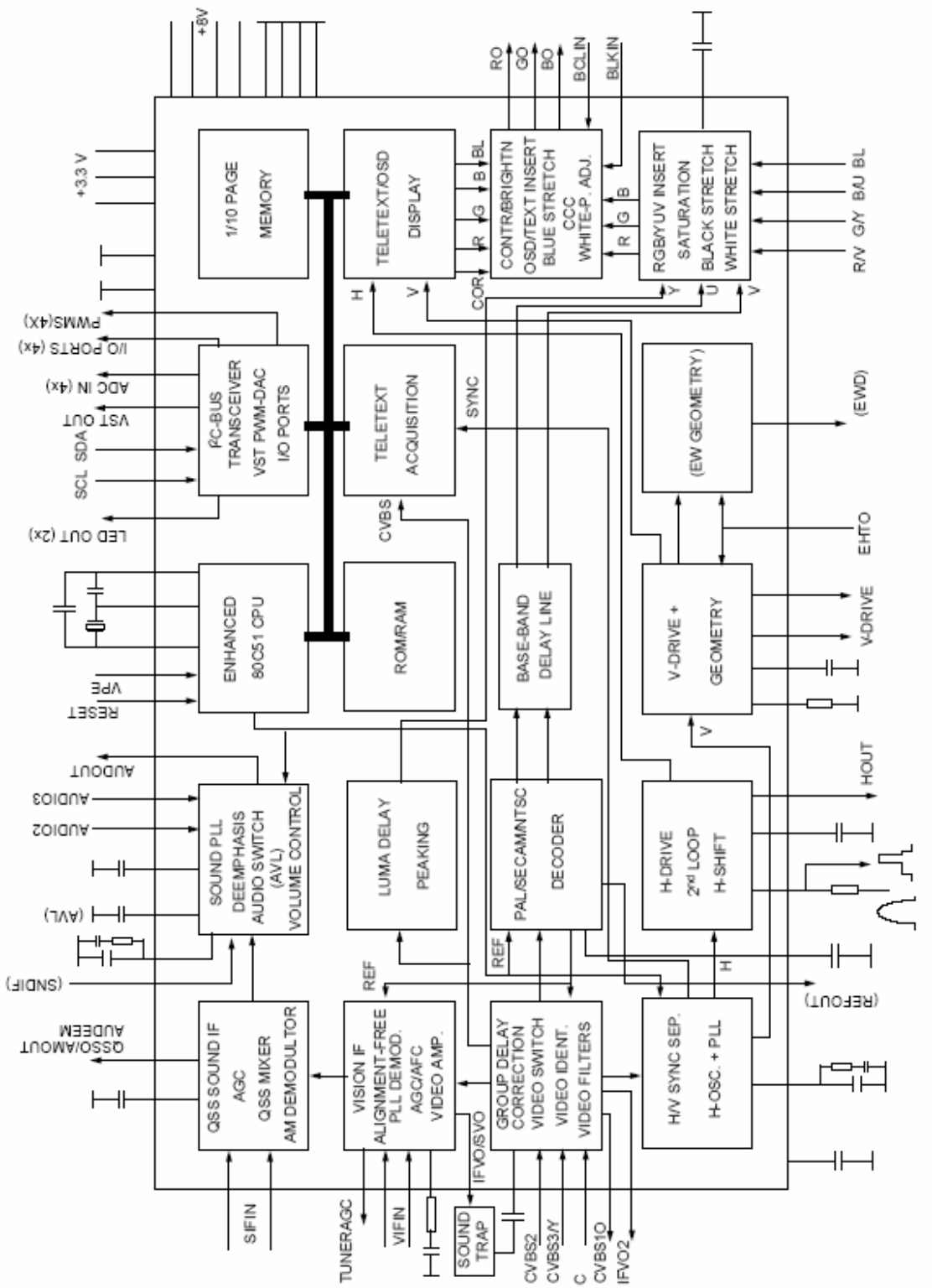
FUNCTIONALOF TDA9552H

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch
- Automatic Volume Levelling
- QSS sound IF amplifier with separate input and AGC circuit
- AM sound demodulator without extra reference circuit
- PAL decoder
- SECAM decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext
- Close Captioning

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltages	–	8.0/3.3	–	V
I_P	supply current (V_P = 8 V)	–	135	–	mA
I_P	supply current (V_P = 3.3 V)	–	60	–	mA
Input voltages					
$V_{iVIFrms)}$	video IF amplifier sensitivity (RMS value)	–	75	–	µV
$V_{iSIF(rms)}$	QSS sound IF amplifier sensitivity (RMS value)	–	60	–	µV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	–	500	–	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	–	1.0	–	V
$V_{iCHROMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
$V_{iY(p-p)}$	luminance input signal (peak-to-peak value)	–	1.4 / 1.0	–	V
$V_{iU(p-p)}$ / $V_{iPB(p-p)}$	U / P_B input signal (peak-to-peak value)	–	–1.33 / +0.7	–	V
$V_{iV(p-p)}$ / $V_{iPR(p-p)}$	V / P_R input signal (peak-to-peak value)	–	–1.05 / +0.7	–	V
Output signals					
$V_{o(IFVO)(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.0	–	V
$V_{o(QSSO)(rms)}$	sound IF intercarrier output in QSS versions (RMS value)	–	100	–	mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output in QSS versions (RMS value)	–	500	–	mV
$V_{o(CVBSO)(p-p)}$	selected CVBS output (peak-to-peak value)	–	2.0	–	V
$I_{o(AGCOUT)}$	tuner AGC output current range	0	–	5	mA
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{oHOUT}	horizontal output current	10	–	–	mA
I_{oVERT}	vertical output current (peak-to-peak value)	1	–	–	mA
I_{oEWD}	EW drive output current	1.2	–	–	mA

BLOCK DIAGRAM



PINING

SYMBOL	PIN	DESCRIPTION
P3.1/ADC1	1	port 3.1 or ADC1 input
P3.2/ADC2	2	port 3.2 or ADC2 input
P3.3/ADC3	3	port 3.3 or ADC3 input
VSSC/P	4	digital ground for µ-Controller core and periphery
P0.5	5	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6/CVBSTD	6	port 0.6 (8 mA current sinking capability for direct drive of LEDs) or Composite video input. A positive-going 1V(peak-to-peak) input is required
VSSA	7	analog ground of Teletext decoder and digital ground of TV-processor
SECPLL	8	SECAM PLL decoupling
VP2	9	2nd supply voltage TV-processor (+8 V)
DECDIG	10	supply voltage decoupling of digital circuit of TV-processor
PH2LF	11	phase-2 filter
PH1LF	12	phase-1 filter
GND3	13	ground 3 for TV-processor
DECBG	14	bandgap decoupling
AVL/EWD (1)	15	Automatic Volume Levelling (90° versions) / E-W drive output (110° versions)
VDRB	16	vertical drive B output
VDRA	17	vertical drive A output
IFIN1	18	IF input 1
IFIN2	19	IF input 2
IREF	20	reference current input
VSC	21	vertical sawtooth capacitor
AGCOUT	22	tuner AGC output
SIFIN1	23	SIF input 1
SIFIN2	24	SIF input 2
GND2	25	ground 2 for TV processor
SNDPLL	26	narrow band PLL filter
AVL/REF0/SNDIF (1)	27	Automatic Volume Levelling / subcarrier reference output / sound IF input
AUDIO2	28	audio 2 input
AUDIO3	29	audio 3 input
HOUT	30	horizontal output
FBISO	31	flyback input/sandcastle output
DECSDEM	32	decoupling sound demodulator
QSSO/AMOUT/ AUDEEM (1)	33	QSS intercarrier output / AM output in stereo applications or deemphasis (front-end audio out) / AM output in mono applications
EHTO	34	EHT/overvoltage protection input
PLLIF	35	IF-PLL loop filter
SIFAGC	36	AGC sound IF
QSSO	37	QSS output
IFVO/SVO	38	IF video output / selected CVBS output
VP1	39	main supply voltage TV processor
CVBS1	40	internal CVBS input
GND	41	ground for TV processor
CVBS2	42	external CVBS2 input

SYMBOL	PIN	DESCRIPTION
GND	43	ground for TV-processor
CVBS3/Y	44	CVBS3/Y input
C	45	chroma input
WHSTR	46	white stretch capacitor
CVBSO	47	CVBS output
AUDOUT /AMOUT[1]	48	audio output /AM audio output (volume controlled)
IFVO2	49	2nd IF video output signal (with or without group delay correction)
INSSW2	50	2nd RGB / YUV insertion input
R2/VIN	51	2nd R input / V (R-Y) input / P_R input
G2/YIN	52	2nd G input / Y input
B2/UIN	53	2nd B input / U (B-Y) input / P_B input
BCLIN	54	beam current limiter input
BLKIN	55	black current input / V-guard input
RO	56	Red output
GO	57	Green output
BO	58	Blue output
VDDA	59	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	60	OTP Programming Voltage
VDDC	61	digital supply to core (3.3 V)
OSCGND	62	oscillator ground supply
XTALIN	63	crystal oscillator input
XTALOUT	64	crystal oscillator output
RESET	65	reset
VDDP	66	digital supply to periphery (+3.3 V)
P1.0/INT1	67	port 1.0 or external interrupt 1 input
P1.1/T0	68	port 1.1 or Counter/Timer 0 input
P1.2/INT0	69	port 1.2 or external interrupt 0 input
P1.3/T1	70	port 1.3 or Counter/Timer 1 input
P1.6/SCL	71	port 1.6 or I^2C-bus clock line
P1.7/SDA	72	port 1.7 or I^2C-bus data line
P2.0/TPWM	73	port 2.0 or Tuning PWM output
P2.1/PWM0	74	port 2.1
P2.2/PWM1	75	port 2.2
P2.3/PWM2	76	port 2.3
P2.4/PWM3	77	port 2.4
P2.5/PWM4	78	port 2.5
SYNC_FILTER	79	CVBS (i.e. P0.6/CVBS) Sync filter input: This pin should be connected to V_{SSA} via a 100 nF capacitor.
P3.0/ADC0	80	port 3.0 or ADC0 input

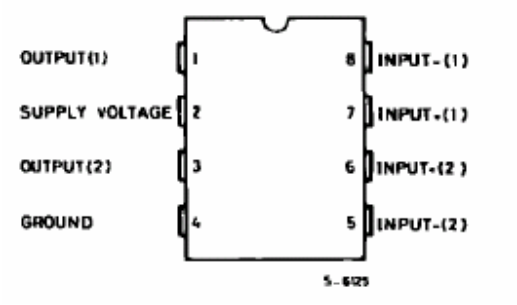
Note

1. The function of pin 15, 27, 33 and 48 is dependent on the mode of operation (mono intercarrier mode / QSS IF amplifier and East-West output or not) and is controlled by some software control bits. The valid combinations are given in table 1.

2.2.2.2. Audio

The TDA2822 is DUAL LOW-VOLTAGE POWER AMPLIFIER.

- Supply voltage down to 1.8V
- Low crossover distorsion
- Low quiescent current
- Bridge or stereo configuration



ELECTRICALCHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		3		15	V
V_c	Quiescent Output Voltage	V_s = 9 V V_s = 6 V		4 2.7		V V
I_d	Quiescent Drain Current			6	12	mA
I_b	Input Bias Current			100		nA
P_o	Output Power (each channel)	d = 10 % f = 1 kHz V_s = 9 V R_L = 4 Ω V_s = 6 V R_L = 4 Ω V_s = 4.5 V R_L = 4 Ω	 1.3 0.45	 1.7 0.65 0.32		 W W W
G_v	Closed Loop Voltage Gain	f = 1 kHz	36	39	41	dB
R_i	Input Resistance	f = 1 kHz	100			kΩ
^eN	Total Input Noise	R_s = 10 kΩ B = 22 Hz to 22 kHz Curve A		 2.5 2		 μV μV
SVR	Supply Voltage Rejection	f = 100 Hz	24	30		dB
CS	Channel Separation	R_g = 10 kΩ f = 1 kHz		50		dB

Figure: Test Circuit (Stereo)

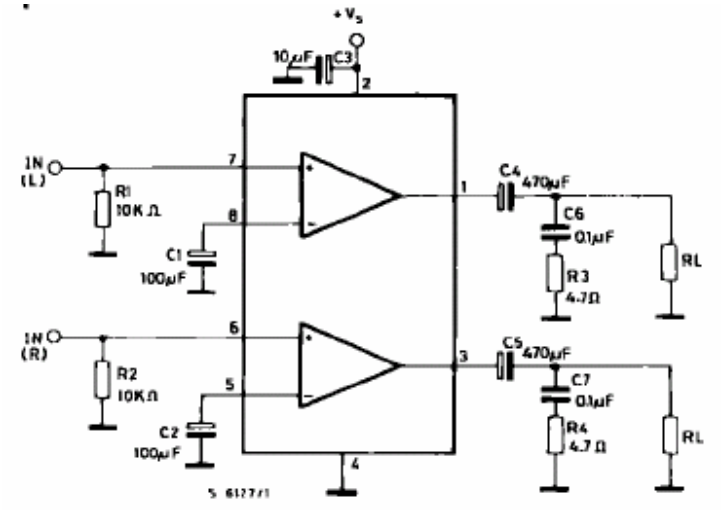


Figure: Test Circuit (Bridge)

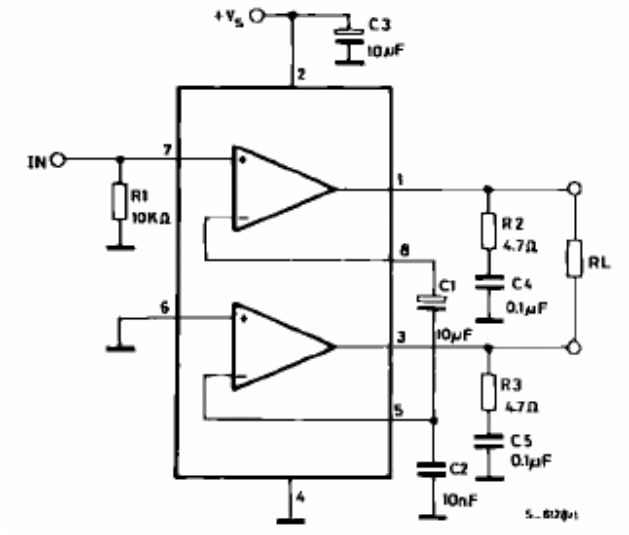
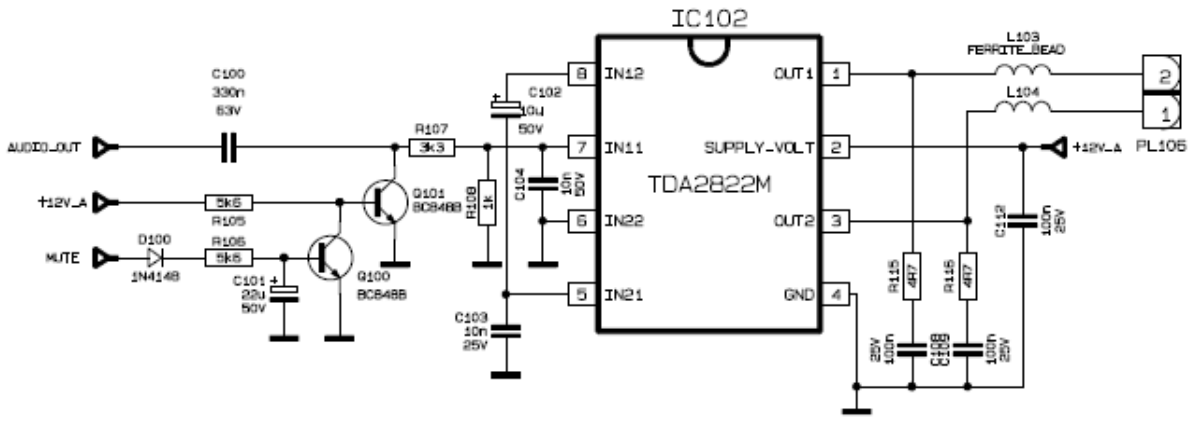


Figure: Application in 11AK56



2.2.2.3. External AV I/O

SCART PINING

1.	Audio right output	0.5Vrms / 1KΩ
2.	Audio right input	0.5Vrms / 10KΩ
3.	Audio left output	0.5Vrms / 1KΩ
4.	Ground AF	
5.	Ground Blue	
6.	Audio left input	0.5Vrms / 10KΩ
7.	Blue input	0.7Vpp / 75Ω
8.	AV switching input	0-12VDC /10KΩ
9.	Ground Green	
10.	Not Used	
11.	Green input	0.7Vpp / 75Ω
12.	Not Used	
13.	Ground Red	
14.	Ground Blanking	
15.	Red input	0.7Vpp / 75Ω
16.	Blanking input	0-0.4VDC, 1-3VDC / 75Ω
17.	Ground CVBS output	
18.	Ground CVBS input	
19.	CVBS output	1Vpp / 75Ω
20.	CVBS input	1Vpp / 75Ω
21.	Ground	

Front/Side/Back AV Input

Audio 0.5Vrms / 10KΩ
Video 1Vpp / 75Ω

Back AV Output

Audio 0.5Vrms / 1KΩ
Video 1Vpp / 75Ω

2.2.2.4. AV Switching

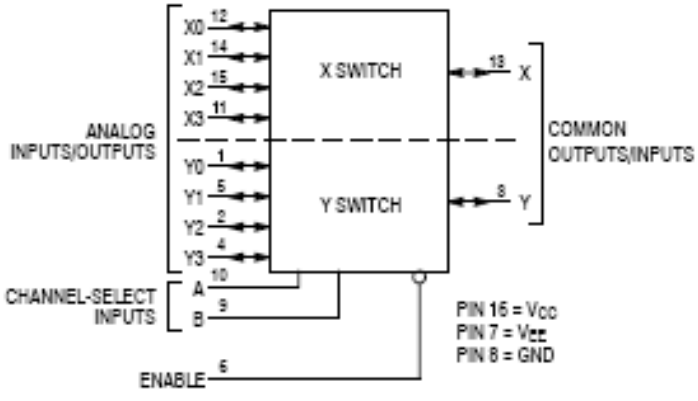
2.2.2.4.1. MC74VHC4052

The MC74VHC4052 utilize silicon--gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from VCC to VEE).

The Channel--Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (Ron) is more linear over input voltage than Ron of metal--gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (VCC -- VEE) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (VCC -- GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal—Gate Counterparts
- Low Noise



MC74VHC4052
Double-Pole, 4-Position Plus Common Off

FUNCTION TABLE – MC74VHC4052

Control Inputs			
Enable	Select B	Select A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})		2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

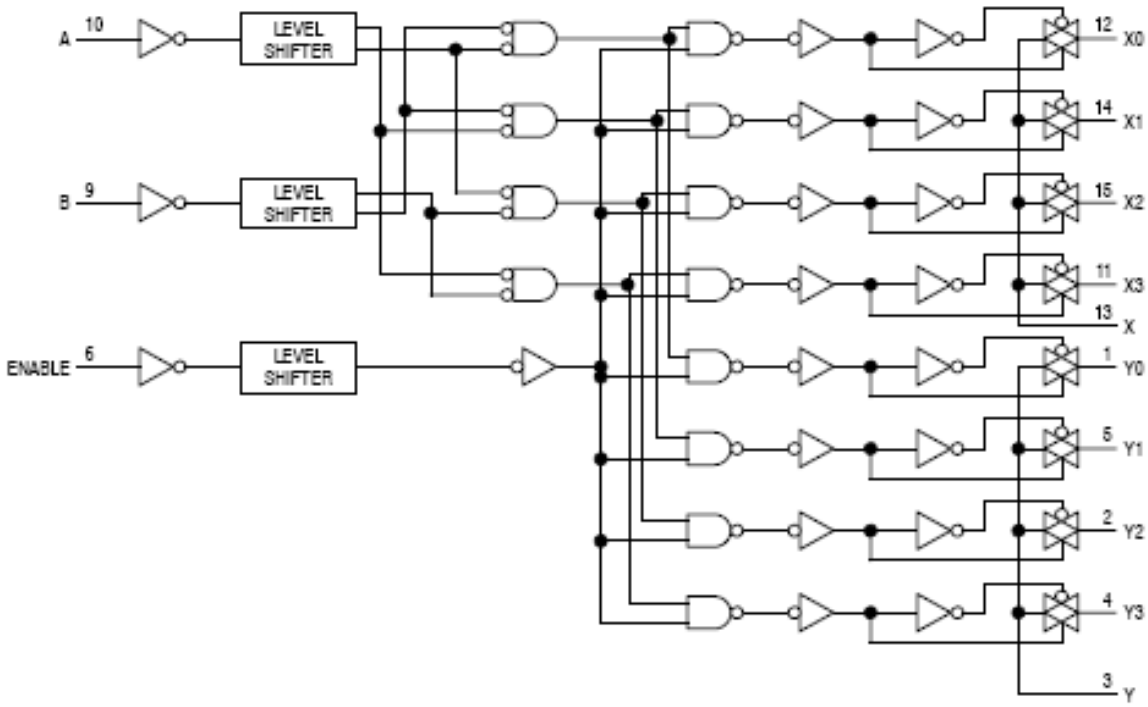


Figure 33. Function Diagram, VHC4052

2.2.2.4.2. NLAST4599

The NLAST4599 is an advanced high speed CMOS single pole – double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power−supply range (from VCC to GND).

The device has been designed so the ON resistance (RON) is much lower and more linear over input voltage than RON of typical CMOS analog switches.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Select Pin Compatible with TTL Levels
- Channel Select Input Over−Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break−Before−Make Circuitry
- Low Power Dissipation: ICC = 2 _A (Max) at TA = 25°C
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch−up Performance Exceeds 300 mA

- ESD Performance: HBM > 2000 V; MM > 200 V
- Chip Complexity: 38 FETs
- Pb−Free Packages are Available

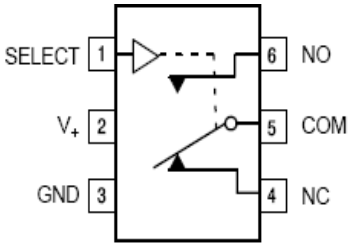


Figure 1. Pin Assignment

FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

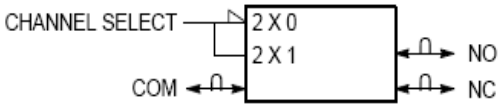


Figure 2. Logic Symbol

MAXIMUM RATINGS (Note 1)

Parameter		Symbol	Value	Unit
Positive DC Supply Voltage		V_{CC}	−0.5 to +7.0	V
Analog Input Voltage (V_{NO} or V_{COM})		V_{IS}	$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
Digital Select Input Voltage		V_{IN}	$-0.5 \le V_I \le +7.0$	V
DC Current, Into or Out of Any Pin		I_{IK}	±50	mA
Power Dissipation in Still Air	SC−88 TSOP6	P_D	200 200	mW
Storage Temperature Range		T_{STG}	−65 to +150	°C
Lead Temperature, 1mm from Case for 10 seconds		T_L	260	°C
Junction Temperature Under Bias		T_J	150	°C
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	2000 200 N/A	V
Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 5)	$I_{LATCHUP}$	±300	mA
Thermal Resistance	SC−88 TSOP6	θ_{JA}	333 333	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22−A114−A
3. Tested to EIA/JESD22−A115−A
4. Tested to JESD22−C101−A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Max	Unit
DC Supply Voltage		V_{CC}	2.0	5.5	V
Digital Select Input Voltage		V_{IN}	GND	5.5	V
Analog Input Voltage (NC, NO, COM)		V_{IS}	GND	V_{CC}	V
Operating Temperature Range		T_A	−55	+125	°C
Input Rise or Fall Time SELECT	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	t_r, t_f	0 0	100 20	ns/V

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V_{CC}	Guaranteed Limit			Unit
				−55 to 25°C	<85°C	<125°C	
Minimum High−Level Input Voltage, Select Input		V_{IH}	3.0 4.5 5.5	2.0 2.0 2.0	2.0 2.0 2.0	2.0 2.0 2.0	V
Maximum Low−Level Input Voltage, Select Input		V_{IL}	3.0 4.5 5.5	0.5 0.8 0.8	0.5 0.8 0.8	0.5 0.8 0.8	V
Maximum Input Leakage Current, Select Input	V_{IN} = 5.5 V or GND	I_{IN}	5.5	±0.1	±1.0	±1.0	μA
Power Off Leakage Current	V_{IN} = 5.5 V or GND	I_{OFF}	0	±10	±10	±10	μA
Maximum Quiescent Supply Current	Select and V_{IS} = V_{CC} or GND	I_{CC}	5.5	1.0	1.0	2.0	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Condition	Symbol	V_{CC}	Guaranteed Limit			Unit
				−55 to 25°C	<85°C	<125°C	
Maximum "ON" Resistance (Figures 17 – 23)	V_{IN} = V_{IL} or V_{IH} V_{IS} = GND to V_{CC} I_{IN}I ≤ 10.0 mA	R_{ON}	2.5 3.0 4.5 5.5	85 45 30 25	95 50 35 30	105 55 40 35	Ω
ON Resistance Flatness (Figures 17 – 23)	V_{IN} = V_{IL} or V_{IH} I_{IN}I ≤ 10.0 mA V_{IS} = 1V, 2V, 3.5V	R_{FLAT} (ON)	4.5	4	4	5	Ω
ON Resistance Match Between Channels	V_{IN} = V_{IL} or V_{IH} I_{IN}I ≤ 10.0 mA V_{NO} or V_{NC} = 3.5 V	ΔR_{ON} (ON)	4.5	2	2	3	Ω
NO or NC Off Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} or V_{NC} = 1.0 V_{COM} 4.5 V	$I_{NC(OFF)}$ $I_{NO(OFF)}$	5.5	1	10	100	nA
COM ON Leakage Current (Figure 9)	V_{IN} = V_{IL} or V_{IH} V_{NO} 1.0 V or 4.5 V with V_{NC} floating or V_{NO} 1.0 V or 4.5 V with V_{NO} floating V_{COM} = 1.0 V or 4.5 V	$I_{COM(ON)}$	5.5	1	10	100	nA

2.2.2.5. TUNER

Channel coverage of PLLTuner for VHF/UHF

BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	E2 to C	48.25 to 82.25 **(1)**	S01 to S08	69.25 to 154.25
Mid Band	E5 to E12	175.25 to 224.25	S09 to S38	161.25 to 439.25
High Band	E21 to E69	471.25 to 855.25 **(2)**	S39 to S41	447.25 to 463.25

(1). Enough margin is available to tune down to 45.25 MHz.
(2). Enough margin is available to tune up to 863.25 MHz.

Noise	Typical	Max.
Low band :	5dB	9dB
Mid band :	5dB	9dB
High band :	6dB	9dB

Gain	Min.	Typical	Max.
All channels :	38dB	44dB	52dB
Gain Taper (of-air channels):			8dB

Noise is typically 6dB for all channels. **Gain** is minimum 38dB and maximum 50dB for all channels.

Terminals for External Connection

NO	TERMINAL NAME	DESCRIPTION
1	AGC	AGC Voltage input
2	NC	No Internal connection
3	SAS	Serial Address Selection
4	SCL	Serial Clock Line
5	SDA	Serial Data Line
6	NC	No Internal connection
7	BP	B+ for Internal IC
8	ADC	Analog/Digital Converter input
9	BT	Tuning Voltage supply
10	IF2	IF output 2
11	IF1	IF output 1
12	ANT	VHF/UHF signal input
13	SUB P/J	VHF/UHF signal output for PIP sub-tuner.

Electrical conditions

PAR	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{B+}	B+ Supply Voltage	4.75	5.0	5.5	V
I_{B+}	B+ Supply Current (LNA OFF)		85	120	mA
	B+ Supply Current (LNA ON)		125	160	mA
V_{AGC}	AGC Input Voltage		4.0	4.5	V
VT	Tuning Supply voltage	30	33	35	V
V_{RIPPLE}	Permissible ripple (20Hz to 500kHz)			5	mV_{P-P}
V_{SCL}	Serial clock input Voltage (see Note1)			5.5	V
V_{SDA}	Serial data input Voltage (see Note1)			5.5	V

2.2.2.6. SAW FILTERS

2.2.2.6.1. K3958M (IF Filter for Video Applications)

Standard

- B/G
- D/K
- I
- L/L'

Pin configuration

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF video filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

2.2.2.6.2. K9656M (IF Filter for Audio Applications)

Standard

- B/G
- D/K
- I
- L/L'

Pin configuration

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L'- NICAM)
- Channel 2 (B/G, D/K, L, I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

2.2.2.6.3. K2966 (IF Filter for Intercarrier Applications)

Standard

- B/G
- D/K

Pin configuration

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF filter with Nyquist slope and sound shelf
- Broad sound shelf for sound carriers at 32,40MHz and 33,40 MHz
- Group delay predistortion

2.2.2.6.4. K2962 (IF Filter for Intercarrier Applications)

Standard

- B/G
- I
- L/L'

Pin configuration

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF filter with two Nyquist slope and sound shelf
- Picture carriers at 33,90 MHz and 38,90 MHz
- Broad sound shelf at 15 dB level for sound carriers at 32,90 MHz and 33,40 MHz
- Constant group delay

2.2.2.6.5. G1975 (IF Filter for Intercarrier Applications)

Standard

- B/G

Pin configuration

1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF filter with Nyquist slope and sound shelf
- Picture carrier at 38.90MHz
- Reduced group delay predistortion as compared with standard B/G, half

2.2.2.7. SMPS

2.2.2.7.1. PRIMARY BLOCK

AC power applied via AC inlet, line filter components prevent chassis from incoming noise of AC line, also prevents AC line against created noises by TV. Bridge rectifier and bulk capacitor converts AC voltage to DC voltage. Applied DC voltage to primary winding is then swicthed via MOSFET by primary controller in a controlled manner.

SMPS controller works on quasi-resonant PWM and gets first supply voltage from AC line (SMPS Controller supply). Controller drives MOSFET according to feedback information supplied by shunt regulator and opto-coupler, according to that information adjusts on-time of MOSFET for required power. After the start-up in normal operation mode SMPS controller is supplied by SMT.

Primary block consist of following main parts,

AC Inlet (PL800),

Fuse (F800),

Varistor (R803),

Line Filter For EMC (C801,L800,C800),

SMPS Controller (IC806),

SMPS Controller supply for first Start-up (R807),

Bridge Rectifier (D820,D821,D822,D823),

Rectifier For SMPS Controller(D803),

Bulk Cap (C809),

Clamping Circuitry (R820, C810, C811, D824),

SMT (Switch Mode Transformer) (TR800),

SMT Driver MOSFET (Q802),

Current Sense Resistor (R828),

Protection Components for MOSFET Failure (D805,D806,R826)

2.2.2.7.1.1. SMPS CONTROLLER (NCP1207)

PWM Current-Mode Controller for Free Running Quasi-Resonant Operation

The NCP1207A combines a true current mode modulator and a demagnetization detector to ensure full borderline/critical Conduction Mode in any load/line conditions and minimum drain voltage switching (Quasi−Resonant operation). Due to its inherent skip cycle capability, the controller enters burst mode as soon as the power demand falls below a predetermined level. As this happens at low peak current, no audible noise can be heard. An internal 8.0 _s timer prevents the free−run frequency to exceed 100 kHz (therefore below the 150 kHz CISPR−22 EMI starting limit), while the skip adjustment capability lets the user select the frequency at which the burst foldback takes place.

The Dynamic Self−Supply (DSS) drastically simplifies the transformer design in avoiding the use of an auxiliary winding to supply the NCP1207A. This feature is particularly useful in applications where the output voltage varies during operation (e.g. battery chargers). Due to its high−voltage technology, the IC is directly connected to the high−voltage DC rail. As a result, the short−circuit trip point is not dependent upon any VCC auxiliary level.

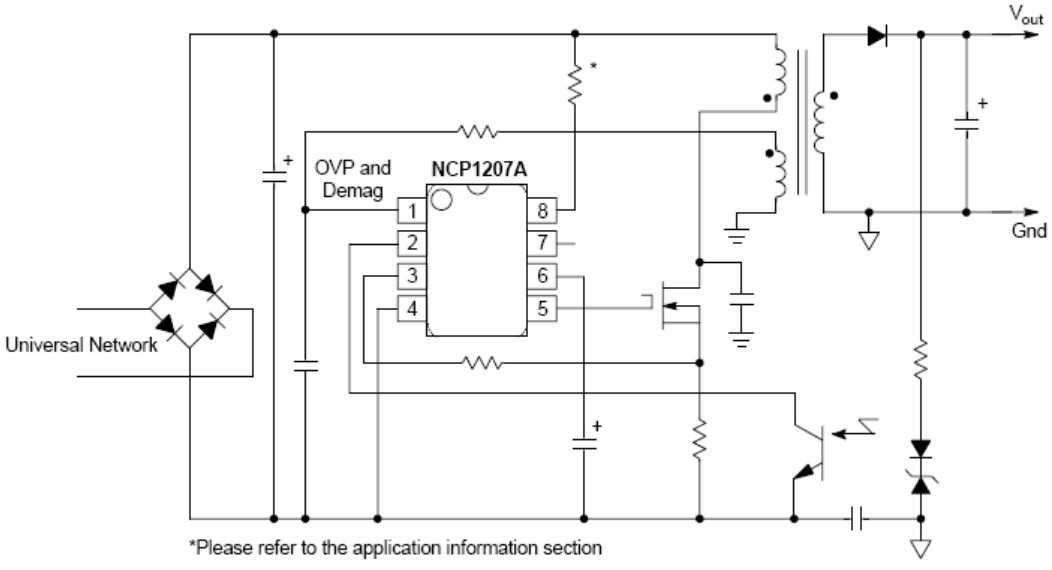
The transformer core reset detection is done through an auxiliary winding which, brought via a dedicated pin, also enables fast Overvoltage Protection (OVP). Once an OVP has been detected, the IC permanently latches off.

Finally, the continuous feedback signal monitoring implemented with an overcurrent fault protection circuitry (OCP) makes the final design rugged and reliable.

Features

- Free−Running Borderline/Critical Mode Quasi−Resonant Operation
- Current−Mode with Adjustable Skip−Cycle Capability
- No Auxiliary Winding VCC Operation
- Auto−Recovery Overcurrent Protection
- Latching Overvoltage Protection
- External Latch Triggering, e.g. Via Overtemperature Signal
- 500 mA Peak Current Source/Sink Capability
- Undervoltage Lockout for VCC Below 10 V
- Internal 1.0 ms Soft−Start
- Internal 8.0 _s Minimum TOFF
- Adjustable Skip Level
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis
- Pb−Free Package is Available Typical Applications
- AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set−Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

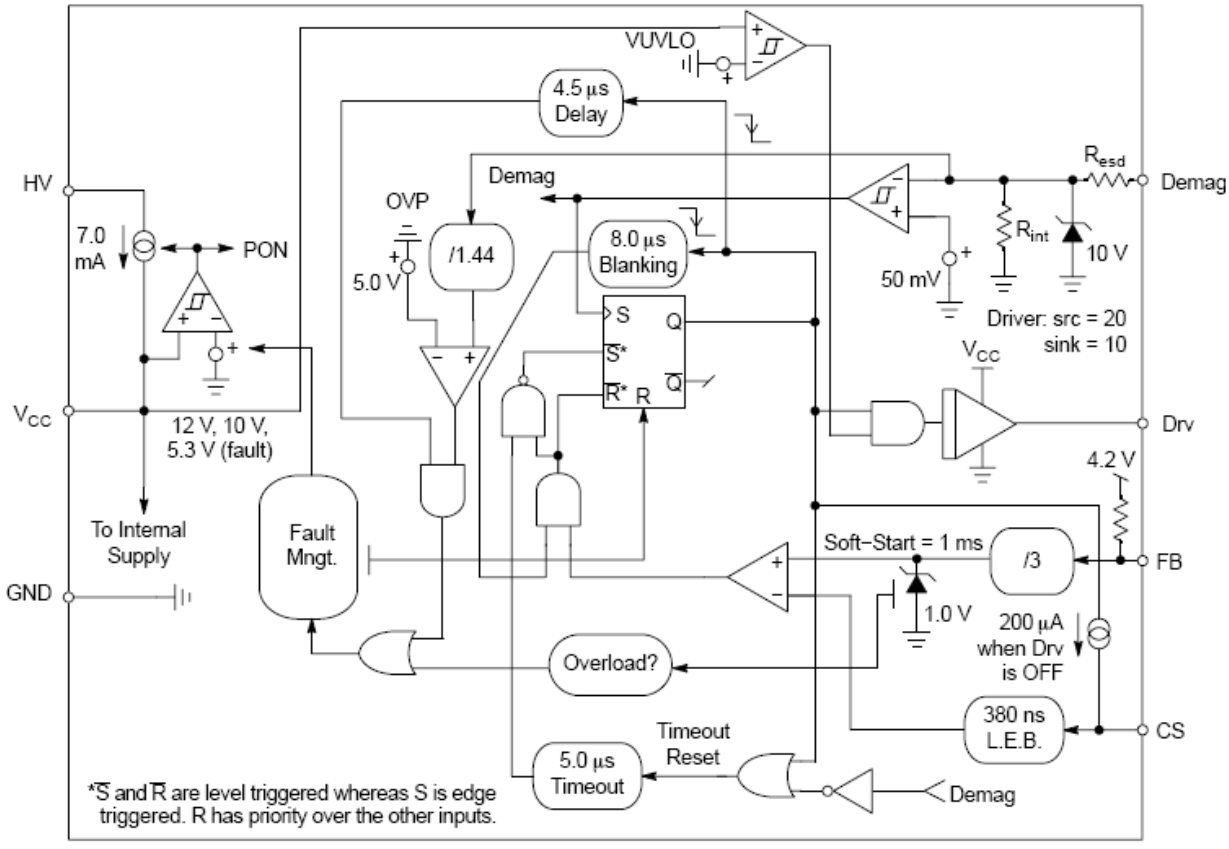
Typical Application:



PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Demag	Core reset detection and OVP	The auxiliary FLYBACK signal ensures discontinuous operation and offers a fixed overvoltage detection level of 7.2 V.
2	FB	Sets the peak current setpoint	By connecting an Optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. By bringing this pin below the internal skip level, device shuts off.
3	CS	Current sense input and skip cycle level selection	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the level at which the skip operation takes place.
4	Gnd	The IC ground	–
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF.
7	NC	–	This unconnected pin ensures adequate creepage distance.
8	HV	High−voltage pin	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.

Internal Circuit Architecture



MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC}, Drv	16	V
Maximum Voltage on all other pins except Pin 8 (HV), Pin 6 (V_{CC}) Pin 5 (Drv) and Pin 1 (Demag)	–	−0.3 to 10	V
Maximum Current into all pins except V_{CC} (6), HV (8) and Demag (1) when 10 V ESD diodes are activated	–	5.0	mA
Maximum Current in Pin 1	Idem	+3.0/−2.0	mA
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	57	°C/W
Thermal Resistance, Junction−to−Air, SOIC version	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction−to−Air, DIP8 version	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	−40 to +125	°C
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	–	155	°C
Hysteresis in Shutdown	–	30	°C
Storage Temperature Range	–	−60 to +150	°C
ESD Capability, HBM Model (All pins except HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMAX}	500	V
Minimum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMIN}	40	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2.2.2.7.1.2. MOSFET

The MTP3N60E used for voltage range 170-270V, The MTP6N60E used for voltage range 90 – 270V.

2.2.2.7.1.2.1. MTP3N60E

N–Channel Enhancement–Mode Silicon Gate

This advanced high voltage TMOS E–FET is designed to with stand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Avalanche Energy Capability Specified at Elevated Temperature
Low Stored Gate Charge for Efficient Switching
Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Pulsed	I_D I_D I_{DM}	3.0 2.4 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

2.2.2.7.1.2.2. MTP6N60E

N–Channel Enhancement–Mode Silicon Gate

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- IDSS and VDS(on) Specified at Elevated Temperature

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 4.6 18	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 9.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	405	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

2.2.2.7.2. SECONDARY BLOCK

Switching primary winding of SMT induces voltages to secondary windings of SMT. Induced voltages are then rectified by secondary recitification diodes and capacitors.

Output Voltages

+3.3.V_STB : The signal is +3.3VDC and continuous stand-by on/off. Used for digital part of UOCII.

+5V_STB : The signal is +5VDC and continuos stand-by on/off. Used for port control.

B+ : The voltage needed for FBT. Voltage range 114V – 117V according to CRT.

12V : The voltage needed for horizantal driver circuit.

12V_A : The voltage supply of audio amplifier.

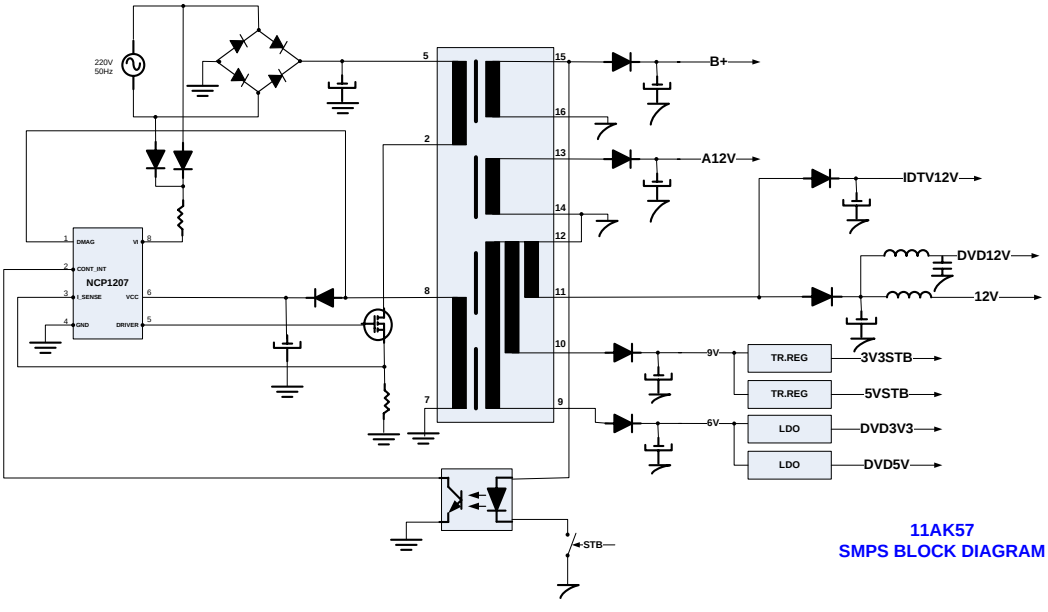
12V_DVD : The voltage needed for DVD.

12V_IDTV : The voltage needed for IDTV.

+5V_DVD : The voltage needed for DVD.

+3.3.V_DVD : The voltage needed for DVD.

2.2.2.7.3. SMPS Block Diagram



11AK57
SMPS BLOCK DIAGRAM

2.2.2.8. DEFLECTION

2.2.2.8.1. HORIZANTAL DEFLECTION

Deflection block consist of following main parts,

Horizontal driver transistor (Q600),
Horizontal driver (L600),
HOT (Horizontal Output Transistor) (Q603),
FBT (TR600),
Linearity Coil (L601),
Flyback Capacitors (C611),
S-correction capacitor (C622),
Modulated S-correction capacitor (C623),
Hdrive signal is buffered and applied to line driver transistor by a capacitor.
Line driver produces necessary base currents, parallel diode to base series resistor speeds up the reverse base current.
UOCII has soft-start and soft-stop features to have more safe operation. There are two base current adjustment resistors on the circuit. Collector current differs according to CRT sizes .
Tube dependent components are choosen to fit best picture performance by keeping;
11-12usec. Flyback time,
Max. 1300V. collector voltage (peak-detect mode measurement)

2.2.2.8.2. MD1803DFX

HIGH VOLTAGE NPN POWER TRANSISTOR FOR STANDARD DEFINITION CRT DISPLAY

Features

- State-Of-The-Art Technology: – Diffused collector "ENHANCED GENERATION"
- More stable performance versus operating temperature variation
- Low base drive requirement
- Tighter hFE range at operating collector current
- Fully insulated power package U.L. compliant
- Integrated free wheeling diode
- In compliance eith the 2002/93/EC EUROPEAN DIRECTIVE

Internal Schematic Diagram

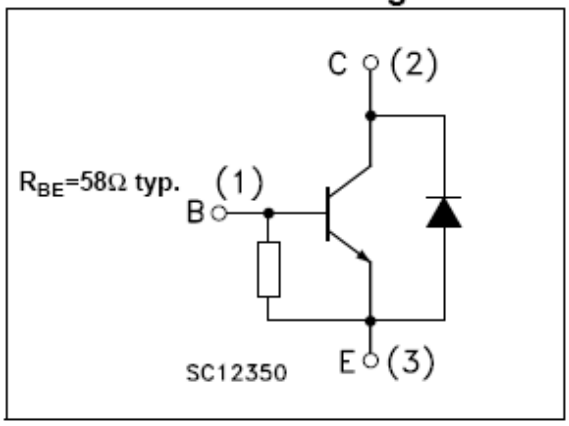


Table 1. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Collector-Base Voltage (I_C = 0)	7	V
I_C	Collector Current	10	A
I_{CM}	Collector Peak Current (t_P < 5ms)	15	A
I_B	Base Current	5	A
P_{TOT}	Total dissipation at T_c = 25°C	57	W
V_{isol}	Insulation Withstand Voltage (RMS) from all three Leads to External Heatsink	2500	V
T_{stg}	Storage Temperature	-65 to 150	°C
T_J	Max. Operating Junction Temperature	150	

Table 2. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	2.2	°C/W

Table 3. **Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500V V_{CE} = 1500V T_c= 125°C			0.2 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5V	75		100	mA
$V_{(BR)EBO}$	Collector-Emitter Breakdown Voltage (I_C = 0)	I_E = 700 mA	7			V
$V_{CE(sat)}$ *Note 1*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A		3	5	V
$V_{BE(sat)}$ *Note 1*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.2	V
h_{FE}	DC Current Gain	I_C = 1 A V_{CE} = 5 V I_C = 5 A V_{CE} = 1 V I_C = 5 A V_{CE} = 5 V	 5	18 5 	 8	
V_f	Diode Forward Voltage	I_F= 5 A		1.5	2	V
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4A f_h = 16KHz $I_{B(on)}$ = 0.6A $V_{BE(off)}$ = -2.5V $L_{BB(off)}$ = 4.5µH		 2.5 0.35		 µs µs

1 Pulsed duration = 300 µs, duty cycle ≤1.5%.

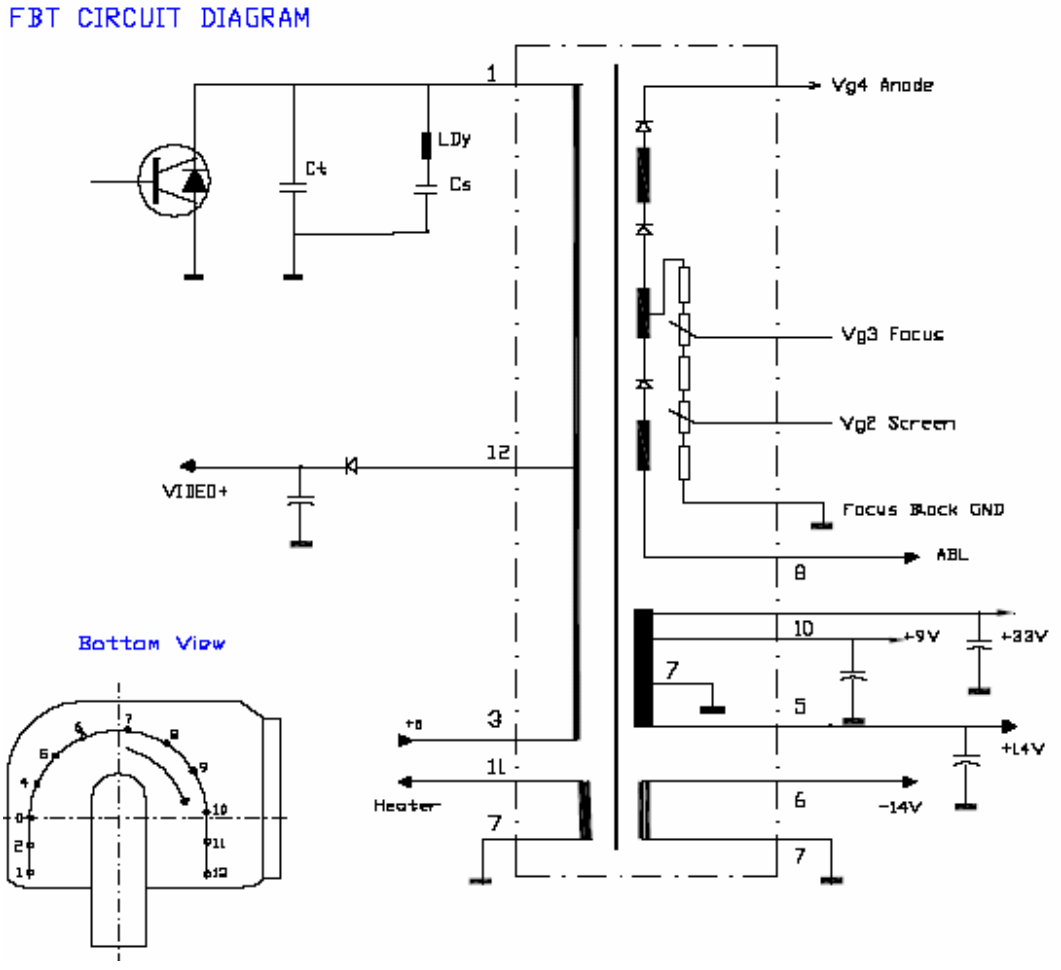
2.2.2.8.3. FBT

Operating Ampient Temperatue : -10°C.....+60°C
Stroge Ampient Temperature : -20°C.....+80°C
Operating Horizantal Frequency : 15.625KHz ±0.5KHz

INDUCTANCE (Between pin1 to pin3) : 3.02mH ± %8
INTERNAL RESISTANCE : Max. 2.2Ohm Regulation:Max.%10
FLYBACK TIME : 11.5µsec
COLLECTOR VOLTAGE : 1000Vp_p
FOCUS VOLTAGE RANGE % OF EHT: min.≤18.2 max.≥34.6
DEFLECTION CURRENT : 3.1Ap_p max.

AUXLIARY OUTPUTS:

Heater Voltage : 6.3Vrms / max 750mA
RGB Supply : +200V / max 30mA ±%5
Vertical Supply : +14V / max 1A ±%5
Vertical Supply : -14V / max 1A ±%5
Auxliary Voltage : +9V / max 1A ±%5
Tuning Voltage : +33V max 100mA ±%5



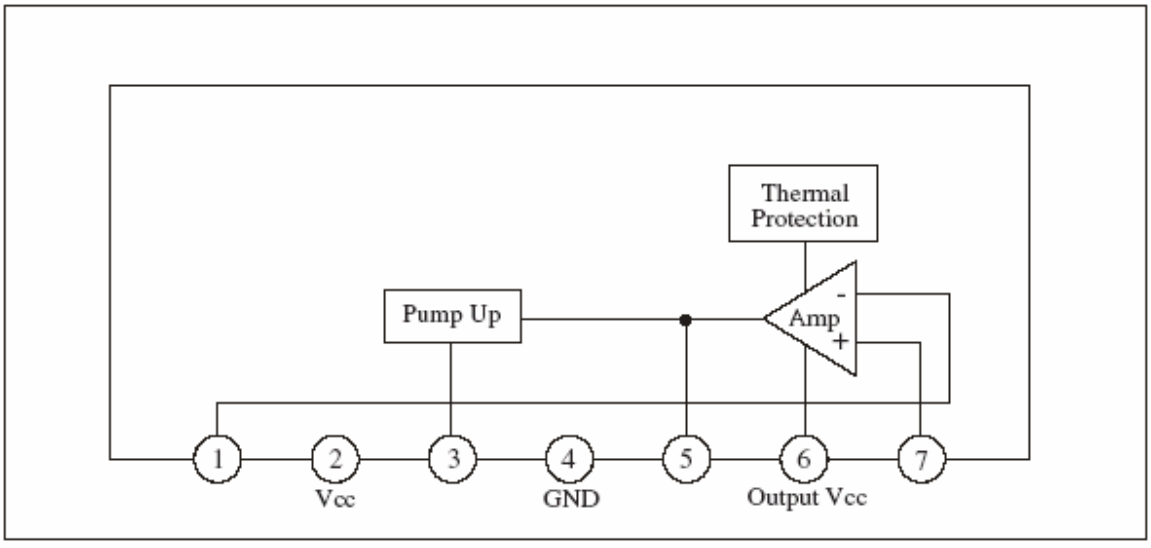
2.2.2.8.4. AN15524A (VERTICAL DEFLECTION OUTPUT)

The AN5524A (TV vertical deflection output circuit) is a monolithic integrated circuit designed for vertical deflection output, such as TV and display.

Features

- Built-in Pump-up circuit
- Built-in Thermal protection circuit
- Maximum deflection current = 1.6Ap-p
- Dimple forming type :
  Advantages : a) Withstand repeated movements between the body and the solder joint of the IC (when a heat-sink is used).
  b) Better vibration absorber (eg. CTV installed in the bus/coach).
- VCC operating range : 12V ~ 30V

■ Block Diagram

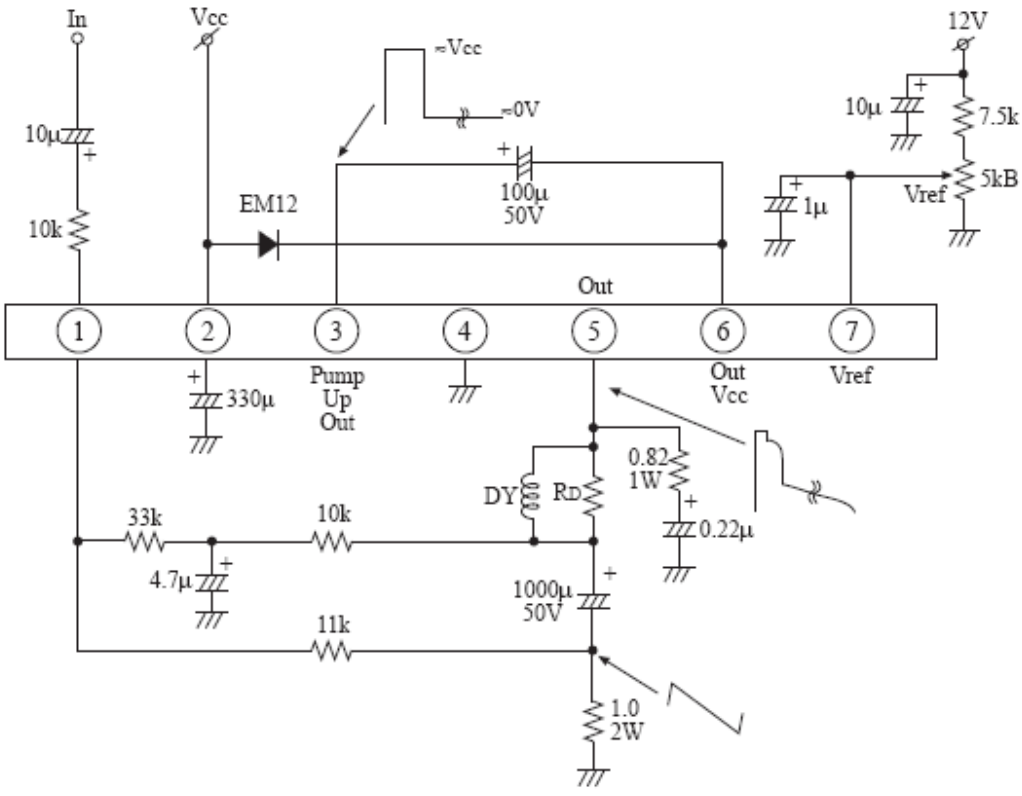


■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating		Unit
Supply Voltage	V_{CC}	30		V
Supply Current	I_{CC}	360		mA
Power Dissipation (Ta=70°C in free air, without heat sink)	P_D	1.5		W
Operating Ambient Temperature	Topr	-20 ~ +70		°C
Storage Temperature	Tstg	-55 ~ +150		°C
Circuit Voltage	V_{5-4}	0	70	V
	V_{6-4}	0	70	
	V_{7-4}	0	V_{2-4}	
	V_{1-4}	0	V_{2-4}	
Circuit Current	I_5	-1.5	1.5	Ao-p
	I_3	-1.1	1.1	

■ Pin

Pin No.	Pin Name
1	Inverting Input
2	V_{CC}
3	Pump-up Output
4	GND
5	Vertical Output
6	Vertical Output Power Supply
7	Non-inverting Input



2.2.2.9. CRT BOARD

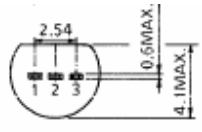
Transistors are used for amplifying RGB signals.

2SC2482 For High Voltage Switching And Amplifier Applications:

- High Voltage : $V_{(BR)}$=300V.
- Small Collector Output Capacitance : C_{ob}=3.0pF (typ.)

MAXIMUM RATINGS (Ta = 25°C)

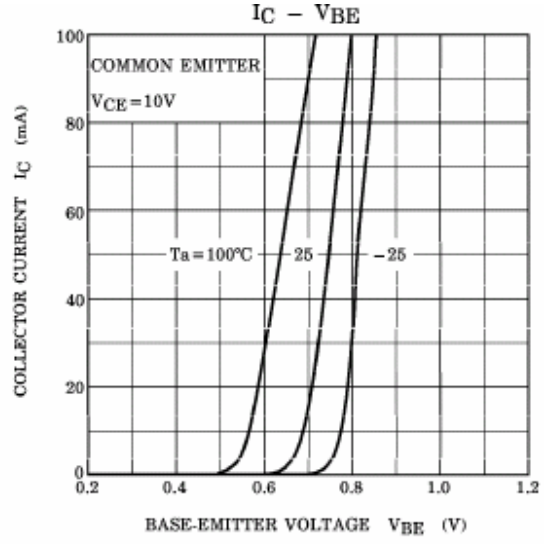
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	300	V
Collector-Emitter Voltage	V_{CEO}	300	V
Emitter-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	100	mA
Base Current	I_B	50	mA
Collector Power Dissipation	P_C	900	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	−55~150	°C

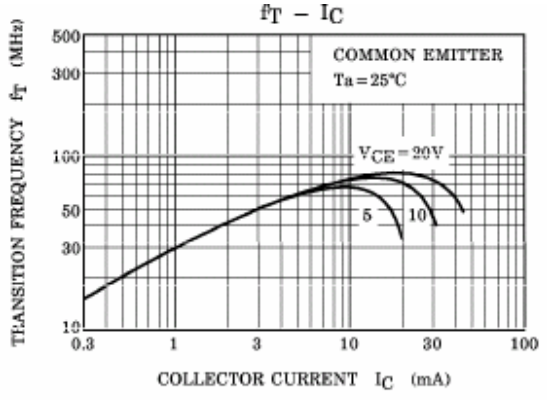


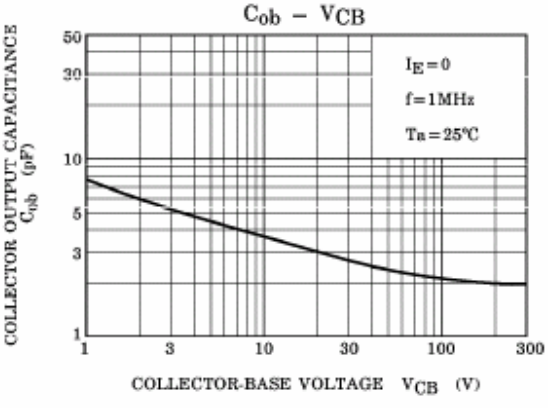
1. EMITTER
2. COLLECTOR
3. BASE

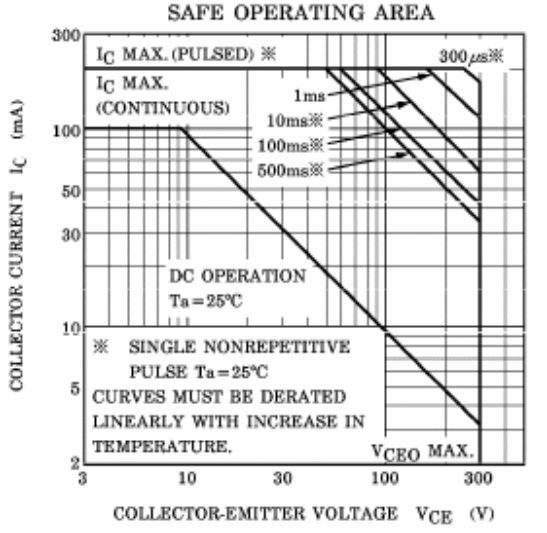
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

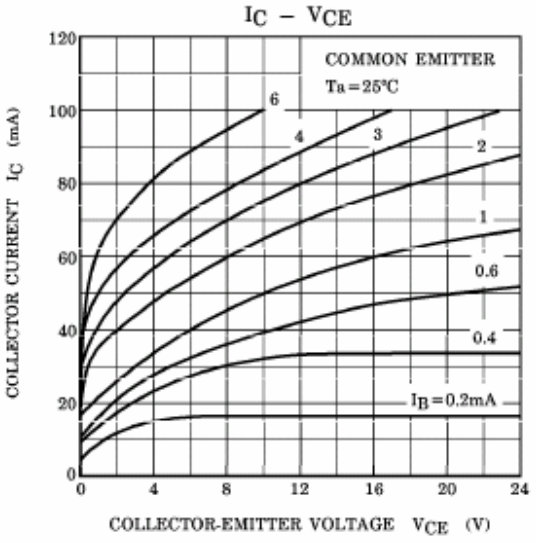
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	V_{CB} = 240V, I_E = 0	—	—	1.0	μA
Emitter Cut-off Current	I_{EBO}	V_{EB} = 7V, I_C = 0	—	—	1.0	μA
DC Current Gain	h_{FE} (1)	V_{CE} = 10V, I_C = 4mA	20	—	—	
	h_{FE} (2)	V_{CE} = 10V, I_C = 20mA	30	—	150	
Collector-Emitter Saturation Voltage	$V_{CE\ (sat)}$	I_C = 10mA, I_B = 1mA	—	—	1.0	V
Base-Emitter Saturation Voltage	$V_{BE\ (sat)}$	I_C = 10mA, I_B = 1mA	—	—	1.0	V
Transition Frequency	f_T	V_{CE} = 10V, I_C = 20mA	50	—	—	MHz
Collector Output Capacitance	C_{ob}	V_{CB} = 20V, I_E = 0, f = 1MHz	—	3.0	—	pF

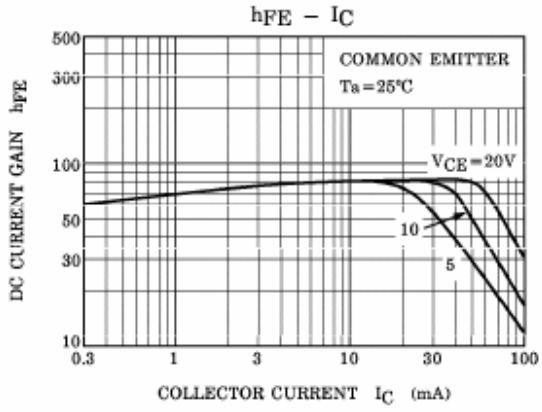


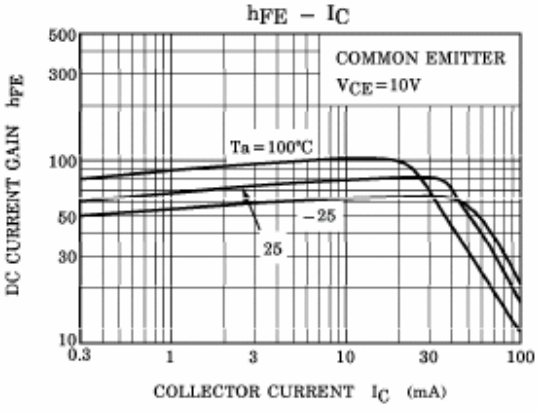


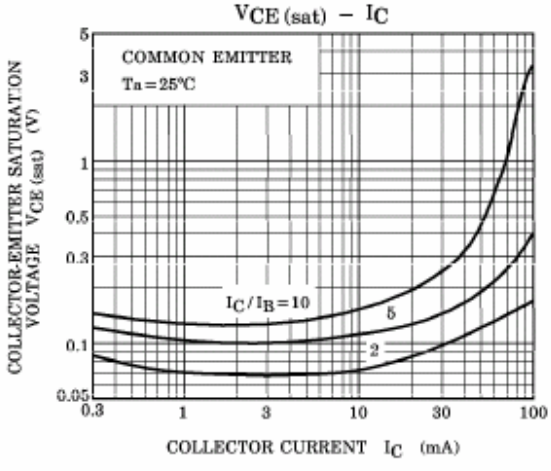


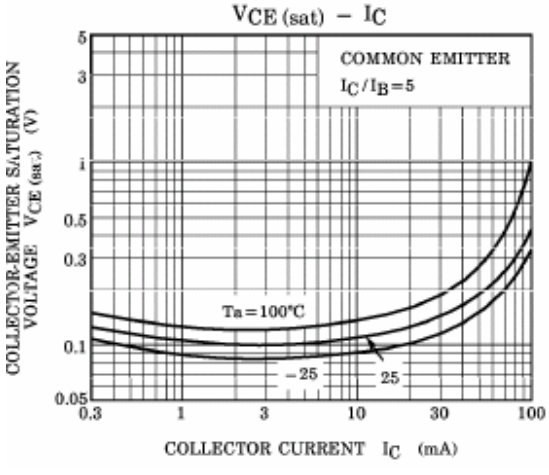


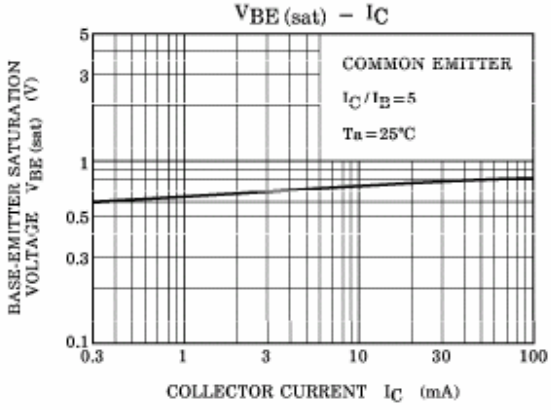

I_C – V_{CE}
COMMON EMITTER
Ta = 25°C
6
4
3
2
1
0.6
0.4
I_B = 0.2mA
COLLECTOR CURRENT I_C (mA)
COLLECTOR-EMITTER VOLTAGE V_{CE} (V)


h_{FE} – I_C
COMMON EMITTER
Ta = 25°C
V_{CE} = 20V
10
5
DC CURRENT GAIN h_{FE}
COLLECTOR CURRENT I_C (mA)


h_{FE} – I_C
COMMON EMITTER
V_{CE} = 10V
Ta = 100°C
25
– 25
DC CURRENT GAIN h_{FE}
COLLECTOR CURRENT I_C (mA)


V_{CE} (sat) – I_C
COMMON EMITTER
Ta = 25°C
I_C / I_B = 10
5
2
COLLECTOR-EMITTER SATURATION VOLTAGE V_{CE} (sat) (V)
COLLECTOR CURRENT I_C (mA)


V_{CE} (sat) – I_C
COMMON EMITTER
I_C / I_B = 5
Ta = 100°C
25
– 25
COLLECTOR-EMITTER SATURATION VOLTAGE V_{CE} (sat) (V)
COLLECTOR CURRENT I_C (mA)


V_{BE} (sat) – I_C
COMMON EMITTER
I_C / I_B = 5
Ta = 25°C
BASE-EMITTER SATURATION VOLTAGE V_{BE} (sat) (V)
COLLECTOR CURRENT I_C (mA)

2.2.3. AK57 Chassis Scematics

2.2.3.1. Part1

VESTEL ELECTRONICS TV R&D GROUP				
001.sht		11AK57 VIDEO&AUDIO		
Ver. 03	Rev.	DATE 08/10/2007	Author YALCIN ELIK	Sheet 01 of 04

TU100 38.9MHz_TVTUN
IF1
IF2/GND
VST
NC/ADC
VS
NC
SDA
SCL
AS
VT
AGC
+33V
+5V
SDA
SCL
PL104
PL105
D101 1N4148
PL102
IRQ
RX
TX
PL103
KEYBOARD
SDA
SCL
+5V_STB
PL106
REMOTE
+5V_STB
PL107
KEYBOARD
LED
PL100
PL101
IC100 24LC02
A0
A1
A2
VSS
VCC
WP
SCL
SDA
IC101 M74HC4052
Y0
Y2
COM_Y_OUT_IN
Y3
COM_X_OUT_IN
Y1
INH
VEE
GND
X2
X1
X0
X3
A
B
IDTV_CVBS
RCA_V_IN
SC_V_IN
DVD_CVBS
IDTV_MONO
SC_A_IN
SW0
SW1
SEL_CVBS
SEL_MONO
IC102 TDA2822M
IN12
IN11
IN22
IN21
OUT1
SUPPLY_VOLT
OUT2
GND
AUDIO_OUT
MUTE
+12V_A
PL108 PL109
IC103
P3.1_ADC1
P3.2_ADC2
P3.3_ADC3
VSSC_P
P0.5
P0.6
VSSA
DEC
VP2
DECDIG
PH2LF
PF1LF
GND3
DECBG
AVL
VDRB
VDRA
HFIN1
HFIN2
IREF
VSC
AGCOUT
IC1
XTALOUT
XTALIN
OSCGND
VDDC
VPE
VDDA
BO
GO
RO
BLKIN
BCLIN
B2_UIN
G2_YIN
R2_VIN
INSSW2
IFVO2
AUDOUT1
CVBS10
WHSTR
CVBS3_Y
GNDA1
CVBS2
GND
RESET
VDDP
P1.0_INT1
P1.1_T0
P1.2_INTO
P1.3_T1
P1.6_SCL
P1.7_SDA
P2.0_PMW
P2.1_PWM0
P2.2_PWM1
P2.3_PWM2
P2.4_PWM3
P2.5_PWM4
NC
P3.0_ADC0
EHT_INFO
+3V3_STB
+8V
VPROT
SC_B_IN
SC_G_IN
SC_R_IN
SC_FBLK
AUDIO_OUT
CVBS_OUT
SEL_CVBS
KEYBOARD
SC_STATUS
LED
SAW_SW
COMMON
VERT+
VERT-
IF1
IF2
IC104 NLAST4599
IC105 NLAST4599
SW0
SW2
DVD_SPDIF
SPDIF_OUT
IDTV_SPDIF
SEL_MONO
RF_MONO
SC_A_OUT
SPDIF_OUT
CVBS1
VP1
SVO_IFOUT
IC2
SIFAGC
PLLIF
EHTO
AUDEEM
DECSDEM
FBISO
HOUT
AUDIO3
AUDIO2
REFOUT_SNDIF
SNDPLL
GND2
HFLYBACK
SEL_MONO
+5V_STB
HOUT
+5V
AGC
RACK_RCA_DVB JK101
PL119
PL111
PL112
PL121
PL113
PL114
PL115
PL116
PL117
PL118
RCA_A_IN
RCA_V_IN
DVD_CVBS
DVD_Q
IDTV_CVBS
IDTV_MONO
DVD_MONO
DVD_SPDIF
IDTV_SPDIF
SC_A_OUT

VESTEL ELECTRONICS	TV R&D GROUP			
002.sht		11AK57 SMPS		
Ver. 03	Rev.	DATE 08/10/2007	Author SMPS GROUP	Sheet 02 of 04

TR800

SMPS_46

IC806

MC44608

IC811

TCET110G

IC812 TL05_TO5

IC813 L4931

IC814 KA78R12

IC815 LM1117

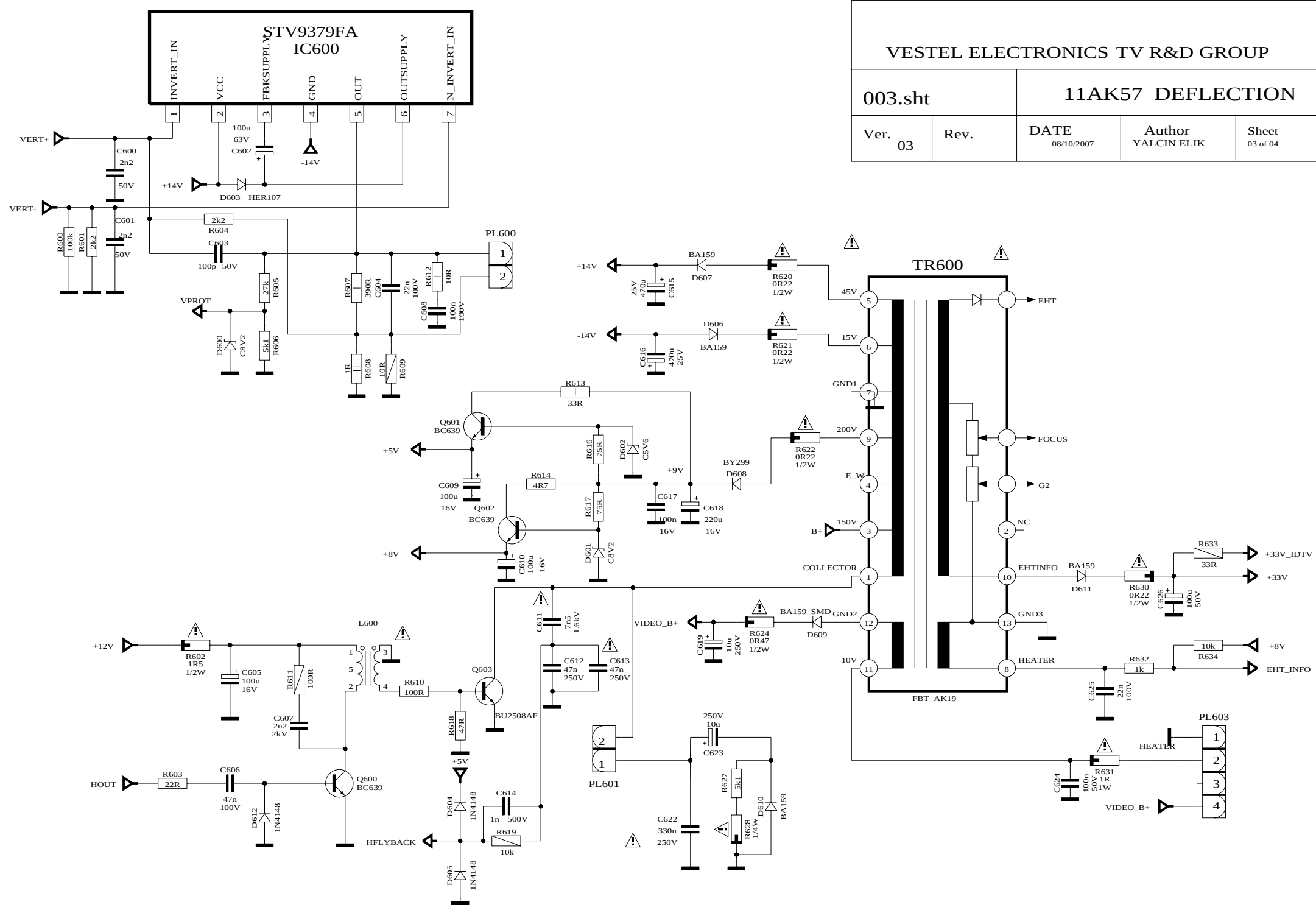
PROTECTION

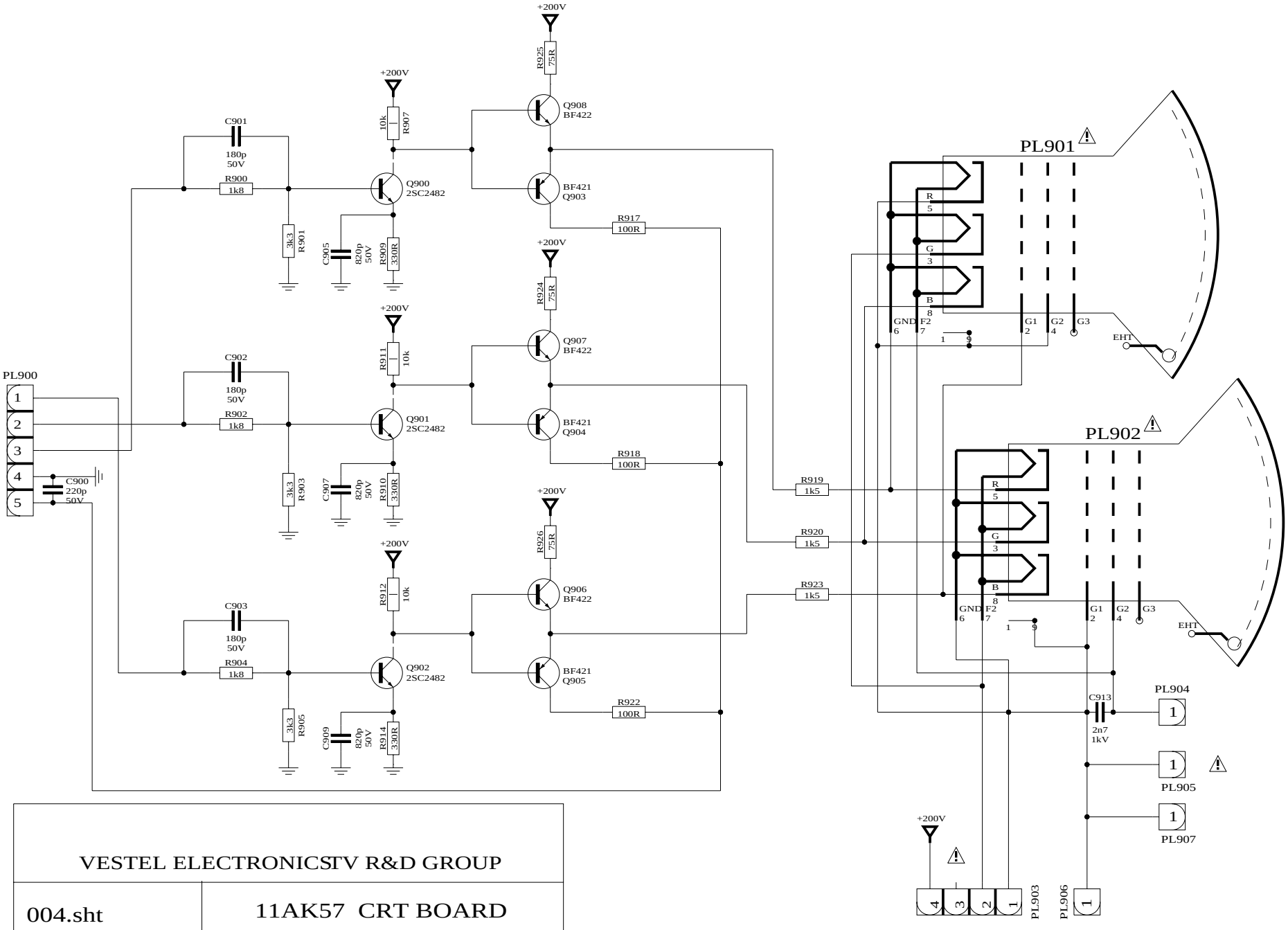
PL800 PL802 PL803 PL804 PL805

RL800

MTP6N60E/SSP7N60A

TL431SAMF2


STV9379FA
IC600
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
VERT+
VERT-
C600 2n2 50V
C601 2n2 50V
R600 100k
R601 2k2
2k2 R604
C603 100p 50V
100u 63V C602
-14V
+14V
D603 HER107
VPROT
27k R605
D600 C8V2
5k1 R606
R607 390R
C604 22n 100V
R612 10R
C608 100n 100V
1R R608
10R R609
PL600
1
2
VESTEL ELECTRONICS TV R&D GROUP
003.sht
11AK57 DEFLECTION
Ver. 03
Rev.
DATE 08/10/2007
Author YALCIN ELIK
Sheet 03 of 04
TR600
+14V
BA159
D607
R620 0R22 1/2W
C615 470u 25V
-14V
D606
BA159
R621 0R22 1/2W
C616 470u 25V
45V
15V
GND1
200V
E_W
150V
B+
COLLECTOR
EHT
FOCUS
G2
NC
EHTINFO
GND2
GND3
HEATER
10V
FBT_AK19
R613 33R
Q601 BC639
+5V
R616 75R
D602 C5V6
+9V
BY299 D608
R622 0R22 1/2W
R614 4R7
C609 100u 16V
Q602 BC639
R617 75R
C617 100n 16V
C618 220u 16V
+8V
C610 100u 16V
D601 C8V2
BA159
D611
R630 0R22 1/2W
C626 100u 50V
R633 33R
+33V_IDTV
+33V
+12V
R602 1R5 1/2W
C605 100u 16V
L600
R611 100R
C607 2n2 2kV
R610 100R
Q603
BU2508AF
R618 47R
C611 7n5 1.6kV
C612 47n 250V
C613 47n 250V
VIDEO_B+
R624 0R47 1/2W
BA159_SMD
D609
C619 10u 250V
10k R634
+8V
EHT_INFO
R632 1k
C625 22n 100V
HOUT
R603 22R
C606 47n 100V
Q600 BC639
D612 1N4148
D604 1N4148
D605 1N4148
C614 1n 500V
R619 10k
HFLYBACK
PL601
250V 10u C623
C622 330n 250V
R627 5k1
R628 1/4W
D610 BA159
PL603
HEATER
R631 1R 1W
C624 100n 50V
VIDEO_B+



VESTEL ELECTRONICSTV R&D GROUP				
004.sht		11AK57 CRT BOARD		
Ver. 03	Rev.	DATE 08/10/2007	Author YALCIN ELIK	Sheet 04 of 04

2.2.4. DVD PLAYER

2.2.4.1. General Description

2.2.4.1.1. MT1389D

The MT1389D Progressive Scan DVD-Player Combo Chip is a single-chip MPEG video decoding chip that integrates audio/video stream data processing, TV encoder, four video DACs with Macrovision. Copy protection, DVD system navigation, system control and housekeeping functions.

The features of this chip can be listed as follows:

Features

- Progressive scan DVD-player combo chip
- Integrated NTSC/PAL encoder.
- Built-in progressive video output
- DVD-Video, VCD 1.1, 2.0, and SVCD
- Unified track buffer and A/V decoding buffer.
- Direct interface of 32-bit SDRAM.
- Servo controller and data channel processing.

Video Related Features:

- Macrovision 7.1 for NTSC/PAL interlaced video.
- Simultaneous composite video and S-video outputs, or composite and YUV outputs, or composite and RGB outputs.
- 8-bit CCIR 601 YUV 4:2:2 output.
- Decodes MPEG video and MPEG2 main profile at main level.
- Maximum input bit rate of 15Mbits/sec

Audio Related Features:

- Dolby Digital (AC-3) and Dolby Pro Logic.
- Dolby Digital S/PDIF digital audio output.
- High-Definition Compatible Digital. (HDCD) decoding.
- Dolby Digital Class A and HDCD certified.
- CD-DA.
- MP3.

2.2.4.1.2. SDRAM Memory Interface

The MT1389D provides a glueless 16-bit interface to DRAM memory devices used as OSD, MPEG stream and video buffer memory for a DVD player. The maximum amount of memory supported is 16MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 110-Mb addressing. The memory interface controls access to both external SDRAM memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

2.2.4.1.3. Drive Interfaces

The MT1389D supports the DV34 interface, and other RF and servo interfaces used by many types of DVD loaders. These interfaces meet the specifications of many DVD loader manufacturers.

2.2.4.2. System Block Diagram and MT1389D Pin Description

2.2.4.2.1. MT1389D Pin Description

Pin	Main	Alt.	Type	Description
RF Interface (26)				
191	RFGND18		Ground	Analog ground
192	RFVDD18		Power	Analog power 1.8V
212	OSP		Analog output	RF Offset cancellation capacitor connecting
213	OSN		Analog output	RF Offset cancellation capacitor connecting
214	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
215	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS.
216	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input
ALPC (4)				

Pin	Main	Alt.	Type	Description
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
26	RFLVL	RFON	Analog output	1) RFRP low pass, or 2) Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE Slicing Level
Analog Servo Interface (8)				
204	ADCVDD3		Power	Analog 3.3V Power for ADC
205	ADCVSS		Ground	Analog ground for ADC
206	RFVDD3		Power	Analog Power
207	RFRPDC		Analog output	RF ripple detect output
208	RFRPAC		Analog Input	RF ripple detect input(through AC-coupling)
209	HRFZC		Analog Input	High frequency RF ripple zero crossing
210	CRTPLP		Analog output	Defect level filter capacitor connecting
211	RFGND		Ground	Analog Power
RF Data PLL Interface (9)				
195	JITFO		Analog output	The output terminal of RF jitter meter.
196	JITFN		Analog Input	The input terminal of RF jitter meter.
197	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry.
198	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
199	PLLVDD3		Power	Power pin for data PLL and related analog circuitry.
200	LPFON		Analog Output	The negative output of loop filter amplifier
201	LPFIP		Analog Input	The positive input terminal of loop filter amplifier.
202	LPFIN		Analog Input	The negative input terminal of loop filter amplifier.
203	LPFOP		Analog Output	The positive output of loop filter amplifier

Pin	Main	Alt.	Type	Description
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output.
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output.
38	FMO		Analog Output	Feed motor control. PWM output.
39	TROPENPWM		Analog Output	Tray PWM output / Tray open output.
40	PWMOUT1	ADIN0	Analog Output	1) 1st General PWM output, or 2) AD input 0
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator.
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
43	FG (Diogital pin)	ADIN1 GPIO	LVTTL 3.3V Input, Schmitt Input, pull up , with analog input path for ADIN1	1) Motor Hall sensor input, or 2) AD input 1, or 3) GPIO
General Power/Ground (27)				
48,84, 133,156	DVDD18		Power	1.8V power pin for internal digital circuitry
71,120, 143	DVSS		Ground	1.8V Ground pin for internal digital circuitry
58,61,87, 108,123,138, 151,168	DVDD3		Power	3.3V power pin for internal digital circuitry
56,74,97, 115,130,145, 160	DVSS		Ground	3.3V Ground pin for internal digital circuitry
184	APLLCAP		Analog Inout	APLL External Capacitance connection
185	APLLVSS		Ground	Ground pin for audio clock circuitry
183	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
Micro Controller and Flash Interface (48)				
54	HIGHA0		Inout 4~16MA, SR PU	Microcontroller address 8
68	HIGHA1		Inout 4~16MA, SR PU	Microcontroller address 9
67	HIGHA2		Inout 4~16MA, SR PU	Microcontroller address 10

Pin	Main	Alt.	Type	Description
66	HIGHA3		Inout 4~16MA, SR PU	Microcontroller address 11
65	HIGHA4		Inout 4~16MA, SR PU	Microcontroller address 12
64	HIGHA5		Inout 4~16MA, SR PU	Microcontroller address 13
63	HIGHA6		Inout 4~16MA, SR PU	Microcontroller address 14
62	HIGHA7		Inout 4~16MA, SR PU	Microcontroller address 15
85	AD7		Inout 4~16MA, SR	Microcontroller address/data 7
81	AD6		Inout 4~16MA, SR	Microcontroller address/data 6
80	AD5		Inout 4~16MA, SR	Microcontroller address/data 5
79	AD4		Inout 4~16MA, SR	Microcontroller address/data 4
78	AD3		Inout 4~16MA, SR	Microcontroller address/data 3
77	AD2		Inout 4~16MA, SR	Microcontroller address/data 2
76	AD1		Inout 4~16MA, SR	Microcontroller address/data 1
75	AD0		Inout 4~16MA, SR	Microcontroller address/data 0
88	IOA0		Inout 4~16MA, SR PU	Microcontroller address 0 / IO
72	IOA1		Inout 4~16MA, SR PU	Microcontroller address 1 / IO
47	IOA2		Inout 4~16MA, SR PU	Microcontroller address 2 / IO
49	IOA3		Inout 4~16MA, SR PU	Microcontroller address 3 / IO
50	IOA4		Inout 4~16MA, SR PU	Microcontroller address 4 / IO

Pin	Main	Alt.	Type	Description
51	IOA5		Inout 4~16MA, SR PU	Microcontroller address 5 / IO
52	IOA6		Inout 4~16MA, SR PU	Microcontroller address 6 / IO
53	IOA7		Inout 4~16MA, SR PU	Microcontroller address 7 / IO
60	A16		Output 4~16MA, SR PU	Flash address 16
86	A17		Output 4~16MA, SR PU	Flash address 17
55	IOA18		Inout 4~16MA, SR PD, SMT	Flash address 18 / IO
57	IOA19		Inout 4~16MA, SR PD, SMT	Flash address 19 / IO
69	IOA20		Inout 4~16MA, SR PD, SMT	Flash address 20 / IO
82	IOA21	GPIO	Inout 4~16MA, SR PD, SMT	1) Flash address 21 / IO 2) While External FLASH size <= 2MB: GPIO
83	ALE		Inout 4~16MA, SR PU, SMT	Microcontroller address latch enable
73	IOOE#		Inout 4~16MA, SR SMT	Flash output enable, active low / IO
59	IOWR#		Inout 4~16MA, SR PU, SMT	Flash write enable, active low / IO
70	IOCS#		Inout 4~16MA, SR SMT	Flash chip select, active low / IO
89	UWR#		Inout 4~16MA, SR PU, SMT	Microcontroller write strobe, active low
90	URD#		Inout 4~16MA, SR PU, SMT	Microcontroller read strobe, active low

Pin	Main	Alt.	Type	Description
91	UP1_2		Inout 4MA, SR PU, SMT	Microcontroller port 1-2
92	UP1_3		Inout 4MA, SR PU, SMT	Microcontroller port 1-3
94	UP1_4		Inout 4MA, SR PU, SMT	Microcontroller port 1-4
95	UP1_5		Inout 4MA, SR PU, SMT	Microcontroller port 1-5
96	UP1_6	SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-6 2) I^2C clock pin
98	UP1_7	SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 1-7 2) I^2C data pin
99	UP3_0	RXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-0 2) 8032 RS232 RXD
100	UP3_1	TXD	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-1 2) 8032 RS232 TXD
101	UP3_4	RXD SCL	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-4 2) Hardwired RD232 RXD 3) I^2C clock pin
102	UP3_5	TXD SDA	Inout 4MA, SR PU, SMT	1) Microcontroller port 3-5 2) Hardwired RD232 TXD 3) I^2C data pin
106	IR		Input SMT	IR control signal input
107	INT0#		Inout 4~16MA, SR PU, SMT	Microcontroller external interrupt 0, active low
Audio interface (14)				
163	ALRCK	GPO	Inout 4MA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I) 1 : use external 373 II) 0: use internal 373 3) While internal AUDIO DAC used: GPO
161	ABCK	GPIO	Inout 4MA	1) Audio bit clock 2) While internal AUDIO DAC used: GPIO

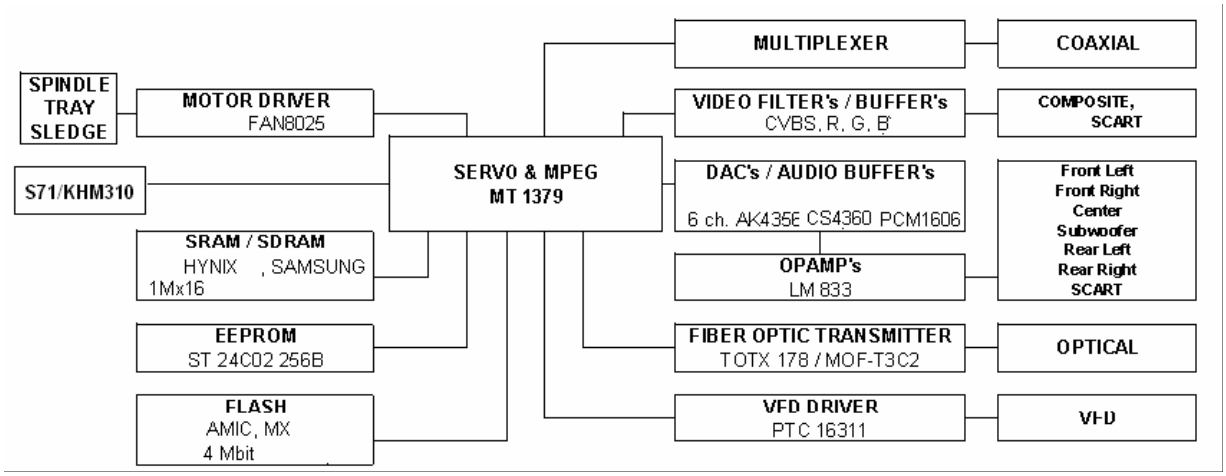
Pin	Main	Alt.	Type	Description
162	ACLK	GPIO	Inout 4MA SMT	1) Audio DAC master clock 2) While internal AUDIO DAC used: GPIO
164	ASDATA0	GPO	Inout 4MA PD SMT	1) Audio serial data 0 (Front-Left/Front-Right) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While internal AUDIO DAC used: GPO
165	ASDATA1	GPO	Inout 4MA PD SMT	1) Audio serial data 1 (Left-Surround/Right-Surround) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While only 2 channels output: GPO
166	ASDATA2	GPO	Inout 4MA PD SMT	1) Audio serial data 2 (Center/LFE) 2) Trap value in power-on reset : I) 1 : manufactory test mode II) 0 : normal operation 3) While only 2 channels output: GPO
167	ASDATA3	GPIO	Inout 4MA PD SMT	1) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 2) While only 2 channels output: GPIO
169	MC_DATA	INT2# GPIO	Inout 2MA	1) Microphone serial input 2) While not support Microphone: I) Microcontroller external interrupt 2 II) GPIO
170	SPDIF		Output 4~16MA, SR : ON/OFF	SPDIF output
186	ADACVDD3		Power	3.3V power pin for AUDIO DAC circuitry
187	AR	GPO	Output	1) AUDIO DAC right channel output 2) While internal AUDIO DAC not used: GPO
188	VCM		Analog	AUDIO DAC reference voltage
189	AL	GPO	Output	1) AUDIO DAC left channel output 2) While internal AUDIO DAC not used: GPO
190	ADACGND		Ground	Ground pin for AUDIO DAC circuitry
Video Interface (12)				
171	DACVDDC		Power	3.3V power pin for VIDEO DAC circuitry
172	VREF		Analog	Bandgap reference voltage
173	FS		Analog	Full scale adjustment
174	DACVSSC		Ground	Ground pin for VIDEO DAC circuitry
175	CVBS		Output 4MA, SR	Analog composite output
176	DACVDDB		Power	3.3V power pin for VIDEO DAC circuitry
177	DACVSSB		Ground	Ground pin for VIDEO DAC circuitry
178	DACVDDA		Power	3.3V power pin for VIDEO DAC circuitry

Pin	Main	Alt.	Type	Description
179	Y/G		Output 4MA, SR	Green or Y or SY or CVBS
180	DACVSSA		Ground	Ground pin for VIDEO DAC circuitry
181	B/CB/PB		Output 4MA, SR	Blue or CB/PB or SC
182	R/CR/PR		Output 4MA, SR	Red or CR/PR or CVBS or SY
MISC (10)				
105	PRST#		Input PU, SMT	Power on reset input, active low
104	ICE		Input PD, SMT	Microcontroller ICE mode enable
193	XTALO		Output	27M crystal out
194	XTALI		Input	27M crystal in
44	GPIO0	VSYN	Inout 4MA, SR SMT	1) General purpose IO 0 2) Vertical sync for video-input
45	GPIO1	HSYN INT4#	Inout 4MA, SR SMT	1) General purpose IO 1 2) Horizontal sync for video-input 3) Microcontroller external interrupt 4
46	GPIO2		Inout 2MA	General purpose IO 2
157	GPIO3	INT1#	Inout 2MA	1) General purpose IO 3 2) Microcontroller external interrupt 1
158	GPIO4		Inout 2MA	General purpose IO 4
159	GPIO5	INT3#	Inout 2MA	1) General purpose IO 5 2) Microcontroller external interrupt 3
93	GPIO6		Inout 4MA, SR PD, SMT	General purpose IO 6
103	GPIO7		Inout 4MA, PD, SMT	General purpose IO 7
Dram Interface (38) (Sorted by position)				
155	RA4		Inout	DRAM address 4
154	RA5		Inout	DRAM address 5
153	RA6		Inout	DRAM address 6
152	RA7		Inout	DRAM address 7
150	RA8		Inout	DRAM address 8
149	RA9		Inout	DRAM address 9
148	RA11		Inout Pull-Down	DRAM address bit 11

Pin	Main	Alt.	Type	Description
147	CKE		output	DRAM clock enable
146	RCLK		Inout	Dram clock
144	RA3		Inout	DRAM address 3
142	RA2		Inout	DRAM address 2
141	RA1		Inout	DRAM address 1
140	RA0		Inout	DRAM address 0
139	RA10		Inout	DRAM address 10
137	BA1		Inout	DRAM bank address 1
136	BA0		Inout	DRAM bank address 0
135	RCS#		output	DRAM chip select, active low
134	RAS#		output	DRAM row address strobe, active low
132	CAS#		output	DRAM column address strobe, active low
131	RWE#		output	DRAM Write enable, active low
129	DQM1		Inout	Data mask 1
128	RD8		Inout	DRAM data 8
127	RD9		Inout	DRAM data 9
126	RD10		Inout	DRAM data 10
125	RD11		Inout	DRAM data 11
124	RD12		Inout	DRAM data 12
122	RD13		Inout	DRAM data 13
121	RD14		Inout	DRAM data 14
119	RD15		Inout	DRAM data 15
118	RD0		Inout	DRAM data 0
117	RD1		Inout	DRAM data 1
116	RD2		Inout	DRAM data 2
114	RD3		Inout	DRAM data 3
113	RD4		Inout	DRAM data 4
112	RD5		Inout	DRAM data 5
111	RD6		Inout	DRAM data 6
110	RD7		Inout	DRAM data 7
109	DQM0		Inout	Data mask 0

2.2.4.2.2. 2.1 Sytem Block Diagram

A sample system block diagram for the MT1389D DVD player board design is shown in the following figurre:



2.2.4.3. Audio Output

The MT1389D supports two-channel and six-channel analog audio output. In a system configuration with six analog outputs, the front left and right channels can be configured to provide the stereo (2 channel) outputs and Dolby Surround, or the left and right front channels for a 5.1 channel surround system. The MT1389D also provides digital output in S/PDIF format. The board supports both optical and coaxial SPDIF outputs.

2.2.4.4. Audio DACS

The MT1389D supports several variations of an I2S type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or LSB first) is possible using the MT1389D internal configuration registers. The I2S format uses four stereo data lines and three clock lines. The I2S data and clock lines can be connected directly to one or more audio DAC to generate analog audio output. The two-channel DAC is internal. The six channel DAC is PCM1606. The outputs of the DACs are not differential. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering.

2.2.4.5. Video Interface

Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the MT1389D. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4: 2:2 to YUV4: 2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Video Post-Processing

The MT1389D video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal upsampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

2.2.4.6. Flash Memory

The decoder board supports 70ns Flash memories.

FLASH_512K_8b

The MT1389D permits 8- bit common memory I/O accesses.

2.2.4.7. Serial Eeprom Memory

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

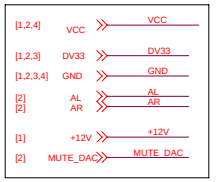
2.2.4.8. Audio Interface Audio Sampling Rate and PLL Component Configuration

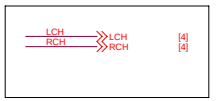
The MT1389D audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I2S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I2S format while six channels Dolby Digital (5.1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I2S interface supports the 112, 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

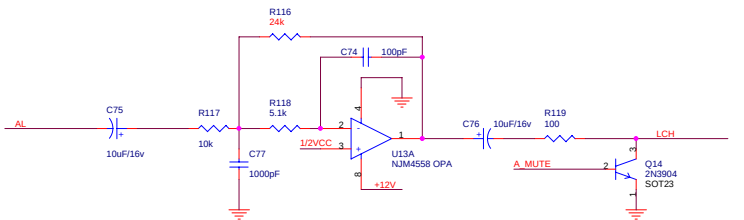
For Linear PCM audio stream format, the MT1389D supports 48 kHz and 96 kHz. Dolby Digital audio only upports 48 kHz. The MT1389D incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock. The MCLK pin is for the audio DAC clock and can either be an output from or an input to the MT1389D. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the MT1389D based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

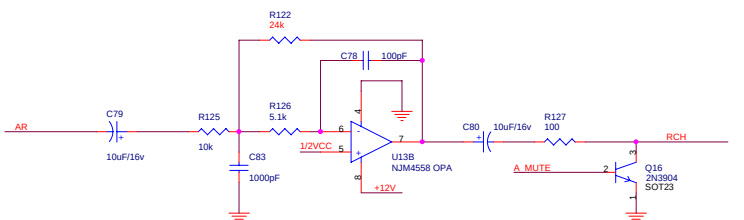
2.2.4.9. Scematics

2.2.4.9.1. Part1

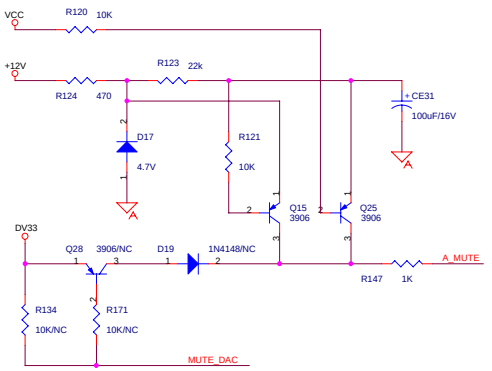


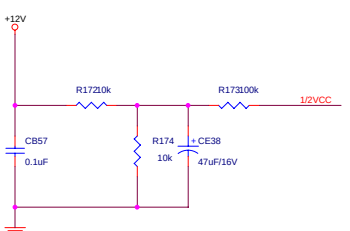


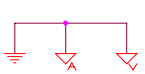




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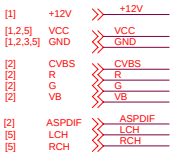


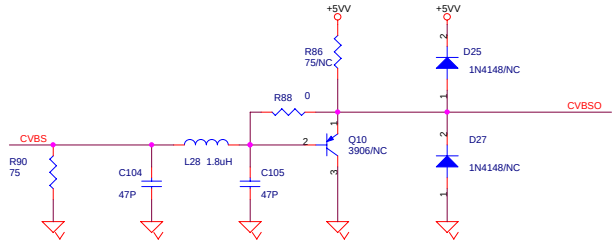


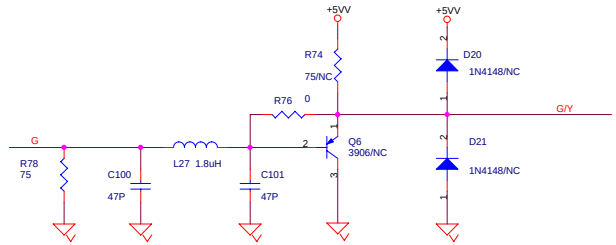
MediaTek Confidential

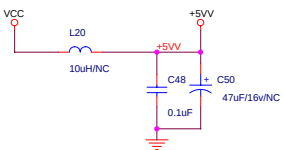
MediaTek (ShenZhen) Inc.

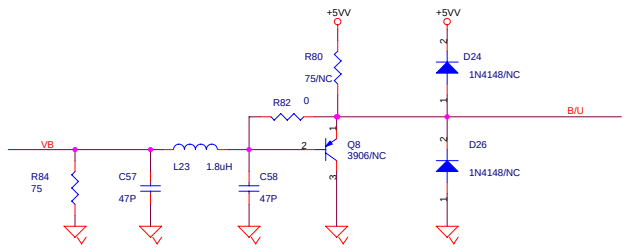
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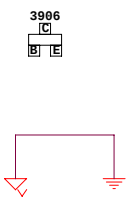


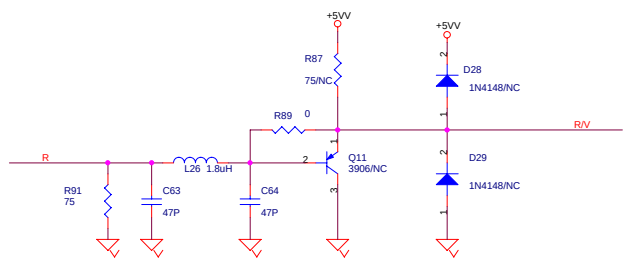


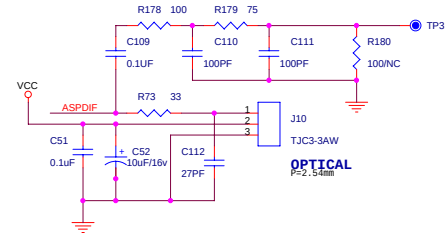


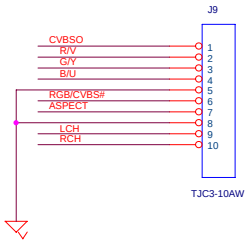


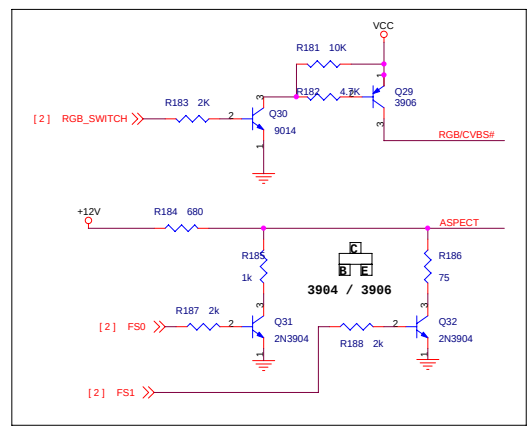












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Size: Custom	Document Number: VIDEO OUT	Drawn: changqiao	Rev: 3
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[1,2,5] DV33 → DV33
[1,2,4,5] GND → GND

DRAM
[2] MA[0..11] → MA[0..11]
[2] BA[0..1] → BA[0..1]
[2] DQM[0..1] → DQM[0..1]
[2] DCLK → DCLK
[2] DCKE → DCKE
[2] CAS# → CAS#
[2] RAS# → RAS#
[2] WE# → WE#
[2] CS# → CS#

FLASH
[2] PCE# → PCE#
[2] PRD# → PRD#
[2] PWR# → PWR#
[1] VCC → VCC
[2] A[0..20] → A[0..20]

DRAM
[2] DQ[0..15] → DQ[0..15]

FLASH
[2] AD[0..7] → AD[0..7]

IIC
[2,3] SCL → SCL
[2,3] SDA → SDA

U8
ESMT M12L64164A/N.C
TSOP54

U7
ESMT M12L16161A-7

RN1
33x4
DCS# 7 8 CS#
DRAS# 5 6 RAS#
DCAS# 3 4 CAS#
DWE# 1 2 WE#

DBA0 R60 33 BA0
DBA1 R61 33 BA1
SDCKE R62 33 DCKE
SDCLK R63 33 DCLK
C107 10PF

DV33 L29 FB SD33
CE25 47uF/16v
CB38 0.1uF
CB39 0.1uF
CB40 0.1uF
CB41 0.1uF
CB42 0.1uF
CB43 0.1uF
CB44 0.1uF
CB45 0.1uF
CB46 0.1uF
CB47 0.1uF

16Mb
A20 R64 0/NC AA20

U9
IC FLASH MX29LV800 8Mb

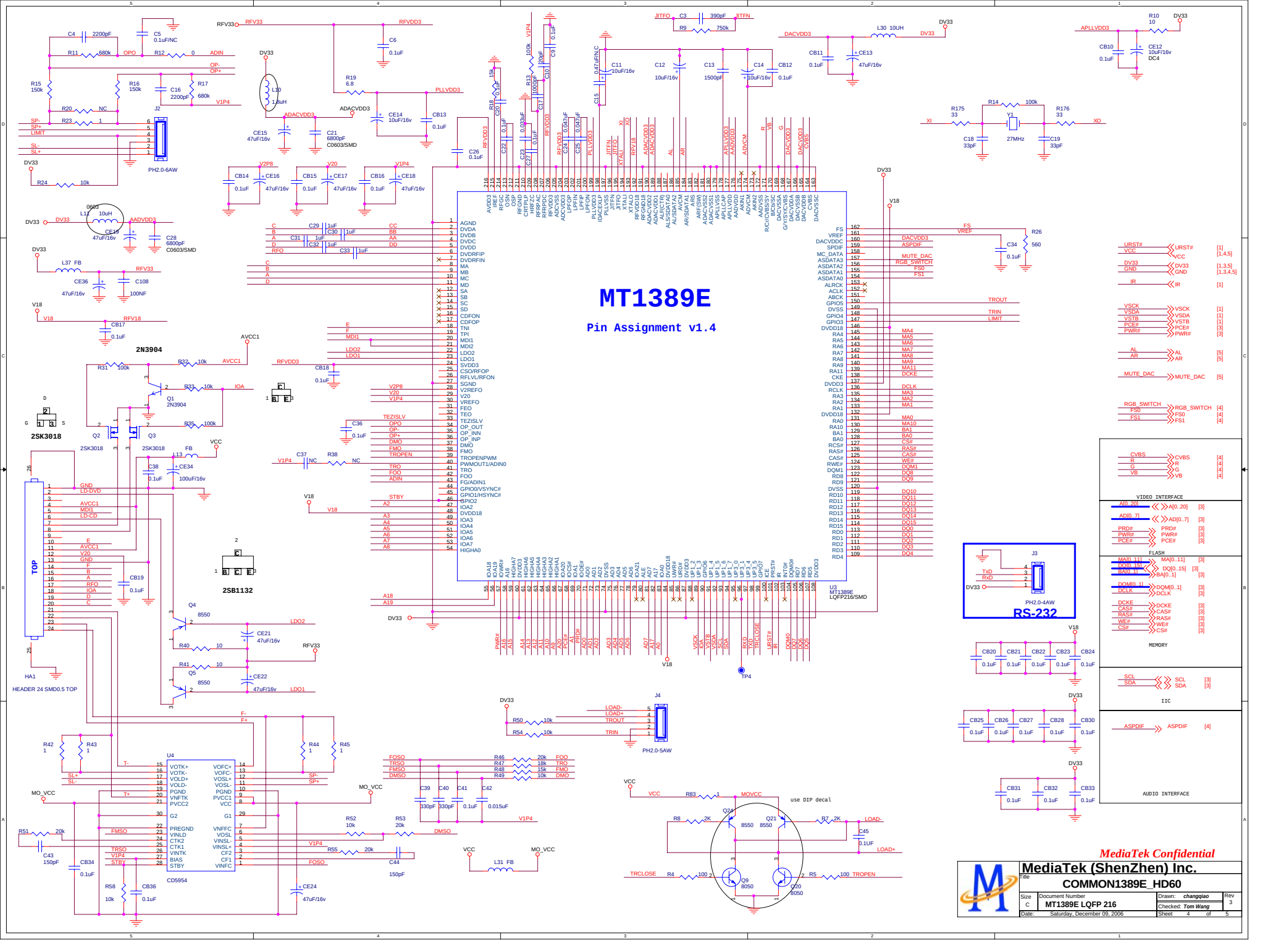
DV33 R85 0 CE26 10uF/16v CB50 0.1uF CB52 0.1uF FVCC
FVCC R68 10k R70 10k
PCE# PRD# PWR#
CB53 0.1uF

U11
EEPROM 24C02
SOP8
DV33 R67 1k R65 1k
GND SCL SDA

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Size: B	Document Number: SDRAM&FLASH	Drawn: changqiao	Rev: 3
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MT1389E
Pin Assignment v1.4
U3
MT1389E
LQFP216/SMD
2N3904
2SK3018
2SB1132
CD5954
PH2.0-6AW
PH2.0-4AW
PH2.0-5AW
HEADER 24 SMD0.5 TOP
RS-232
use DIP decal
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MediaTek (ShenZhen) Inc.
COMMON1389E_HD60
MT1389E LQFP 216
changqiao
Tom Wang
Saturday, December 09, 2006

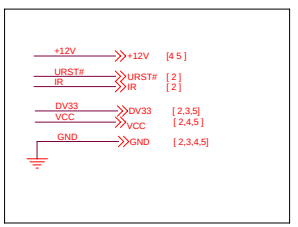
COMMON1389E_HD60_V3

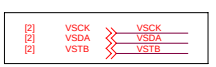
MT1389E (LQFP216) DVD MP Board for SANYO HD60 PUH

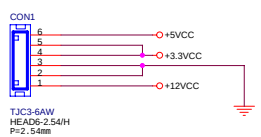
1 INDEX & POWER, RESET
2 MT1389E
3 SDRAM & FLASH
4 VIDEO OUT & AV-CON
5 AUDIO OUT - WM8766

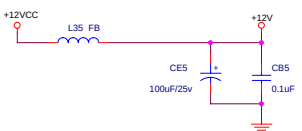
NAME	TYPE	DEVICE
VCC	Digital 5V	SUPPLY
DV33	Digital 3.3V	MT1389E
RFV33	Servo 3.3V	MT1389E
AV33	Laser Diode 3.3V	
V18	Digital 1.8V	MT1389E
SD33	Digital 3.3V	SDRAM
+12V	Audio +12V	OP AMP.
-12V	Audio -12V	OP AMP.
AVDD5	Audio 5V	Audio DAC
DVDD3	Audio 3.3V	Audio DAC

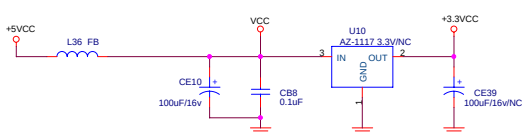
Rev	History	P#	Date
V1	Initial released. Modified from 3-SY1389DP1-V11		2005.01.19
V2	Add SCART and VGA output		2005.03.01
V3	Modify Video backend circuit.		2005.03.09

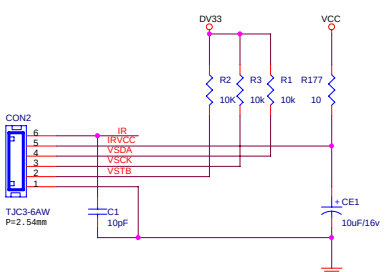


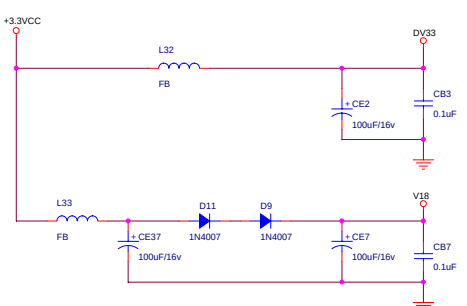




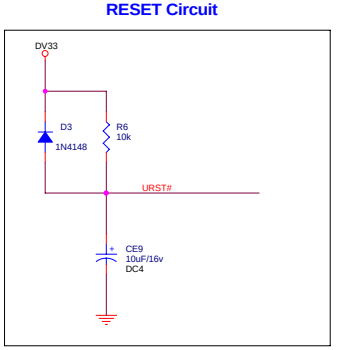








RESET Circuit





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2.3. AK57 Service Menu

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
001	FAPS	First APS	ON = Aktif OFF = İn-Aktif ON = Active OFF = In-active	OFF
002	ISPM	I2C Modu (I2C Mode)	OFF	OFF
003	INIT	Yazılım ve donanım resetleme (Resetting software and hardware)	ON = Resetleme aktif OFF = Resetleme in-aktif ON = Enable resetting OFF = Disable resetting	OFF

Table 1 Init

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
004	AGCSPD	IF AGC hızı (IF AGC speed)	0 = Yavaş 1 = Standart 2 = Hızlı 3 = Hız seviyesi 2' den daha yüksek 0 = Slow 1 = Standard 2 = Fast 3 = Fastest	1
005	AGCTO	AGC Take over	0..63	31

Table 2 AGC Servis ayarları (AGC Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
006	COFF	Cut – Off Ayarı (Cut-Off setting)	0..63	32

Table 3 VG2 Alignment Servis ayarları (VG2 Alignment Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
007	VERT SLOP	Dikey eğim (VSL), SBL biti yarı blank'e anahtarlanmalıdır. (Vertical slope (VSL), SBL bit should be keyed to half-blank.)	0..63	32
008	SCORRECTION	S-doğrulaması (SC) (S-correction (SC))	0..63	32
009	VERT SHIFT	4:3 Wide Screen için dikey kaydırma (4:3 vertical shifting for Wide Screen)	0..63	32
010	VERT AMP	Dikey genlik (VA) (Vertical Amplitude (VA))	0..63	32
011	HOR SHIFT	Yatay kaydırma (Horizontal shifting)	0..63	32
012	VERT SHIFT16	16:9 Wide Screen için dikey kaydırma (16:9 vertical shifting for Wide Screen)	0..63	32
013	VERT AMP16	16:9 Dikey genlik (16:9 Horizontal amplitude)	0..63	32
014	RGB HSH	50 Hz'lik RGB modunda yatay kaydırma (In RGB mode with 50 Hz, horizontal shifting)	0..63	37
015	RGB HSH60	60 Hz'lik RGB modunda yatay kaydırma (In RGB mode with 60 Hz, horizontal shifting)	0..63	37
016	60HZ HSH 43	4:3 MODE 60 Hz yatay kaydırma (In 4:3 MODE with 60 Hz, horizontal shifting)	0..63	31
017	60HZ VSH 43	4:3 MODE 60 Hz dikey kaydırma (In 4:3 MODE with 60 Hz, vertical shifting)	0..63	31
018	60HZ VA 43	4:3 MODE 60 Hz dikey genlik (In 4:3 MODE with 60 Hz, vertical amplitude)	0..63	31
019	60HZ VSH 169	16:9 MODE 60 Hz dikey kaydırma (In 16:9 MODE with 60 Hz, vertical shifting)	0..63	31
020	60HZ VA 169	16:9 MODE 60 Hz Dikey genlik (In 16:9 MODE with 60 Hz, vertical amplitude)	0..63	31

Table 4 Geometri Servis ayarları (Geometry Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
021	QSS	Qss amfi mode değiştirici (Switching the mode of the QSS amplifier)	ON = QSS Aktif OFF = QSS İn-aktif ON = QSS Active OFF = QSS In-Active	ON
022	OIF	IF-PLL'de DC ofset doğrultması (DC offset correction at IF-PLL)	0..63	29
023	IF	PLL demodulatör frekansı (PLL demodulator frequency)	0 = 58.75 MHz 1 = 45.75 MHz 2 = 38.90 MHz 3 = 38.00 MHz 4 = 33.40 MHz 5 = 42.00 MHz 6 = 33.90 MHz 7 = 48.00 MHz 8 = EXTERNAL	2
024	OFR	Frekans Girişi Aktivasyonu: Installation menüsündeki Tuning Mode olan Frekans modunu aktif veya pasif hale getirir. (Frequency Entry Activation: Frequency mode which is value Tuning Mode item on the Installation menu can be enabled or disabled by OFR.)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-Active	ON
025	FFI	IF-PLL Hız filtresi (Fast filter IF-PLL)	ON =Hızlı zaman sabiti OFF = Normal zaman sabiti ON = Fast time constant OFF = Normal time constant	OFF
026	BS1	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..15	1
027	BS2	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..15	2
028	BS3	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..15	4
029	CB	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..255	142

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
030	B1-H	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..255	12
031	B1-L	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..255	32
032	B2-H	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..255	30
033	B2-L	(Gerekli ayarlamayı yapmak için ilgili Tuner dökümanına bakılmalıdır.) (Please look at the related Tuner specification for necessary adjustments.)	0..255	2

Table 5 Tuning Servis ayarları (Tuning Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
034	FRAV	AV için Peaking merkezi frekansı (For AV, Peaking center frequency)	0 = 2.7 Mhz 1 = 3.1 Mhz 2 = 3.5 Mhz	1
035	YSCM	SECAM için Y-delay ayarı (For SECAM, Y-delay setting)	0..15	12
036	YNTS	NTSC için Y-delay ayarı (For NTSC, Y-delay setting)	0..15	2
037	YPAL	PAL için Y-delay ayarı (For PAL, Y-delay setting)	0..15	2
038	YAV1	AV-1 için Y-delay ayarı (For AV-1, Y-delay setting)	0..15	4
039	YSVHS	SVHS için Y-delay ayarı (For S-VHS-2, Y-delay setting)	0..15	4

Table 6 Video Servis ayarları (Video Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
040	WPRC	Cold için White point Red	0..63	32

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
		(For Cold, White point Red)		
041	WPGC	Cold için White point Green (For Cold, White point Green)	0..63	32
042	WPBC	Cold için White point Blue (For Cold, White point Blue)	0..63	31
043	BLORB	Black seviyesi ofset Red – Blue (Black level offset Red – Blue)	0..63	32
044	BLOG	Black seviyesi ofset Green (Black level offset Green)	0..63	32
045	WPRN	Normal için White point Red (For Normal, White point Red)	0..63	37
046	WPGN	Normal için White point Green (For Normal, White point Green)	0..63	32
047	WPBN	Normal için White point Blue (For Normal, White point Blue)	0..63	19
048	BLRB-RGB	RGB için Black seviyesi ofset Red – Blue (For RGB, Black level offset Red – Blue)	0..63	32
049	BLG-RGB	RGB için Black seviyesi ofset Green (For RGB, Black level offset Green)	0..63	32
050	WPRW	Warm için White point Red (For Warm, White point Red)	0..63	49
051	WPGW	Warm için White point Green (For Warm, White point Green)	0..63	40
052	WPBW	Warm için White point Blue (For Warm, White point Blue)	0..63	25
053	BLRB-YUV	YUV için Black seviyesi ofset Red – Blue (For YUV, Black level offset Red – Blue)	0..63	32
054	BLG-YUV	YUV için Black seviyesi ofset Green (For YUV, Black level offset Green)	0..63	32
055	WPRW-RGB	RGB için White point Red (For RGB, White point Red)	0..63	32
056	WPGW-RGB	RGB için White point Green (For RGB, White point Green)	0..63	40
057	WPBW-RGB	RGB için White point Blue (For RGB, White point Blue)	0..63	32

Table 7 White ton ayarları (White tone adjustments)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
058	OSO	Dikey overscan'de Switch-off (Switch-off at vertical overscan)	ON = Aktif Switch-off OFF = İn-aktif Switch-off ON = Enable Switch-off OFF = Disable Switch-off	ON
059	FSL	Dikey sync için Forced Slicing seviyesi (For vertical sync, Forced Slicing level)	ON = Sync genliği %60'ı sabit seviyede bulunan dikey slicing OFF = Otomatik dikey slicing seviyesi ON = Vertical slicing level fixed to 60% of sync amplitude OFF = Automatic vertical slicing level	OFF
060	PN8-STB	If option is ON TV can open from stanby when PIN8 is activated	OFF = feature is not avaliable ON = feature is avaliable	OFF
061	PWL	Peak white sınırlayıcı (Peak white limiting)	0..15	8
062	BPS	Bypass chroma temel-band (Bypass chroma base-band)	ON = Bypass temel-band kroma gecikme çizgisi OFF = Temel-band kroma gecikme çizgisi aktif ON = Bypass baseband chroma delay line OFF = Baseband chroma delay line active	OFF
063	CLPL	Soft kırpma seviyesi (Soft clipping level)	0 = PWL'in 0% üstünde 1 = PWL'in 5% üstünde 2 = PWL'in 10% üstünde 3 = İn-aktif 0 = 0% above PWL 1 = 5% above PWL 2 = 10% above PWL 3 = Off	0
064	CL	Katot drive seviyesi (Cathode drive level)	0..15	10
065	ST-LMI	Option for sleep timer last minute indicator	ON = last minute indicator appears on TV OFF = last minute indicator does not appear on TV	OFF

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
066	DNMENU	Dynamic Menu Mode	ON = Dynamic Menu Enable OFF = Dynamic Menu Disable	OFF
067	UK-EU	IDTV UK veya PAN-EU	OFF = 0 UK (IDTV UK) ON = 1 PAN-EU (IDTV PAN-EU)	OFF

Table 8 Bit Kontrol Servis ayarları (8 Bit Control Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
068	FAVI	FAV (FAV)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	ON
069	BAVI	BAV (BAV)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	OFF
070	BSVI	SVHS (SVHS)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	OFF
071	SSTDBG	BG ses standardı (BG sound standard)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	ON
072	SSTDI	I ses standardı (I sound standard)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	ON
073	SSTDDK	DK ses standardı (DK sound standard)	ON = Aktif OFF = İn-aktif ON = Active OFF = In-active	ON
074	SSTDL	L- L prime ses standardı (L- L prime sound standard)	ON = Aktif OFF = İn-aktif ON = Active	ON

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
			OFF = In-active	

Table 9 Kaynak seçimi Servis seçenekleri (Source Switching Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
075	TXHPOS	Teletext tek sayfa başlangıç noktası ayarları (One page Teletext starting point setting)	0..20	10
076	TXTBRI	Teletext parlaklık ayarı (Teletext brightness setting)	0..63	32
077	TXTCON	Teletext contrast ayarı (Teletext contrast setting)	0..15	0
078	LSEL1	Menü dili seçimi (Menu language setting)	0..255	255
079	LSEL2	Menü dili seçimi (Menu language setting)	0..255	255
080	-------			

Table 10 Teletext Servis seçenekleri (Teletext Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
081	PWPRF	Açılışta görüntü ve sesin gelmesine göre, fast startup ve perfect startup. (According to video and sound, when TV opening, fast startup and perfect startup)	0..15 0 = Fast 15 = Perfect	10
082	PWRES	STANDBY'dan açılır. (Opens from STANDBY.)	ON = Son duruma gore açılır OFF = STANDBY'dan açılır ON = Opens depending on the last state OFF = Opens from STANDBY	ON

Table 11 Güç Servis seçenekleri (Power Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)

083	MAXCOL	Picture menüsündeki maksimum renk ayar sınırlayıcısı (Maximum color setting limiter at Picture menu)	0..63	50
084	MAXBRI	Picture menüsündeki maksimum parlaklık ayar sınırlayıcısı (Maximum brightness setting limiter at Picture menu)	0..63	57
085	MINBRI	Picture menüsndeki minimum parlaklık ayar sınırlaması (Minimum brightness setting limiter at Picture menu)	0..63	20
086	MAXCON	Picture menüsündeki maksimum contrast ayar sınırlayıcısı (Maximum contrast setting limiter at Picture menu)	0..63	50

Table 12 Picture Servis seçenekleri (Picture Service settings)

S-No	OSD	Tanım (Definition)	Mümkün Ayarlar (Possible Settings)	Varsayılan Değer (Default)
087	SAVEFS	Fabrika Servis ayarlarını saklama (Saving Factory settings)	OFF	OFF
088	LOADFS	Fabrika Servis ayarlarını yükleme (Loading Factory setting)	OFF	OFF
089	OAVL	Ses menusunde AVL'i optional yapar (AVL is optional in sound menu) OAVL = 0 (AVL is off and AVL line is not avaliable in sound menu) OAVL = 1 (AVL line is avaliable in sound menu) OAVL = 2 (AVL is on and AVL line is not avaliable in sound menu) Other values of OAVL work like OAVL =1	0-63	32
090	HTLSRC	Selection for hotel mode search HTLSRC = 0 (TV) HTLSRC = 1 (AV) HTLSRC = 2 (FAV) HTLSRC = 3 (SVHS) HTLSRC > 3 (HOTEL MODE NOT AVAILABLE)	0-63	32
091	HMAXVOL	Maximum volume for hotel mode	0-63	32
092	HDEFVOL	Volume level definition for hotel mode when tv is openning	0-63	32
093	RPO	Preover Shoot Ratio PSYS_RATIO_PRE_OVERSHOOT_MIN =0 PSYS_RATIO_PRE_OVERSHOOT_MAX =3	0-3	32

094	PF	Peaking Frequency PF1-PF0 = 0 (2.7 Mhz) 1 (3.1 Mhz) 2 (3.5 Mhz) 3 (spare)	0-3	2
095	APSSND	Default value of sound standard in APS menu 0-> BG 1-> I 2-> DK 3-> L\L'	0-3	0
096	SRCO	Control DVD,IDTV, AV2 (Only AK58) sources 0-> DVD, AV2 are OFF 1-> DVD is ON. AV2 is OFF 2-> AV2 is ON. DVD is OFF 3-> DVD, AV2 are ON	0-7	0

Table 13 Fabrika Servis ayarları (Factory Service settings)

Geometri ayarları : Service menüsündeki 007-011 satırlar arasındaki 50Hz geometri ayarları yapıldıktan sonra, NTSC offsetlerin belirlenmesi için 016-018 satırlar arasındaki NTSC 60Hz ayarları yapılır. NTSC ayarlarını her tüp çalıması için bir kez yapılması yeterlidir. Çünkü NTSC ayarları yapılırken, NTSC offset değerleri hesaplanarak EEPROM da saklanır. 16:9 Zoom modu ayarlarıda NTSC ayarları gibi yapılır ve 16:9 offset değerleri hesaplanarak EEPROM'da saklanır. Daha sonra 50 Hz geometri ayarları değiştirildiğinde, 007-011 veya 016-018 satırlar arasında iken menü tusuna basılarak geometri ayarları kaydedildiğinde, otomatik olarak 16:9 modu, RGB horizontal shift ve NTSC geometri değerleri hesaplanır. RGB horizontal shift offset değerleri koda gömülü haldedir. NTSC ve 16:9 modu offset değeri EEPROM'da saklanmaktadır.

Geometry Adjustment: After adjusting 50Hz geometry items (between 007-011). NTSC 60 Hz geometry items (between 016-018) should be adjusted to determine NTSC 60Hz offset. NTSC offset is automatically calculated and stored in NVM. Later on, if we need to change 50Hz geometry settings, NTSC 60Hz geometry settings is automatically calculated by using NTSC offset. 16:9 mode geometry adjustment works like NTSC 60Hz geometry adjustment.

If press to menu button between 007-011 or 016-018 items. New geometry setting is stored and, 16:9 mode, RGB shift and NTSC geometry automatically calculated. RGB shift offset value is stored in software. Only NTSC offset and 16:9 mode offset values are stored in EEPROM.

AGC ayarı : Tunere 60db yayın verildikten sonra AGCTO iteminin uzerine gelinip mavi tuşa basıldıgında AGC otomatik olarak ayarlanır.

AGC adjustment: Connect to tuner 60db broadcast and, press to blue button on AGCTO item. AGC is automatically adjusted.

Screen Ayarı: Servis menüsünde sarı tuşa basılarak, dikey tarama iptal edilir ve screen ayarının yapılabilmesi için ilgili registerlar güncellenir. Ekranda ince bir çizgi belirir. Daha sonar bu ince çizgi en ince hale gelene kadar screen potansiyometrisi ayarlanır. Tekrar sarı tuşa basıldığında eski ayarlar geri yüklenir.

Screen Adjustment: When yellow button is pressed in service menu. Vertical scan is disabled and related registers are updated. Thin line will be appeared on the screen. Then the screen potentiometer is gently adjusted until the thin line will be lightly disappeared When press to yellow button again, old register values are reloaded and vertical scan is enabled.

FOCUS Ayarı : TV de yayın verilir. . FOCUS potansiyometresi en uygun değerede ayarlanır.

FOCUS Adjustment: TV is tuned to the signal. Then focus potantiometer (the upper pot on the rear side of the FBT transformer) is adjusted for optimum focusing drive.

2.4. TUNER SETTINGS

	VHF1-VHF3	VHF3-UHF	AK56 SERVICE MENU ITEMS							
	Frq. (Mhz)	Frq. (Mhz)	B1-H	B1-L	B2-H	B2-L	BS1	BS2	BS3	CB
Philips UV1316S MK3	156,25 MHz	441,25 MHz	012	050	030	02	001	002	004	142
LG TAEW-G002D	140,25 Mhz	431.25 Mhz	011	050	029	098	001	002	008	142
Thomson CTT5020	114,25 MHz	401,25 MHz	009	146	027	130	003	006	133	142
Samsung TECC2949PG28B	170,25 MHz	465,25 MHz	013	018	031	130	001	002	004	142
Samsung TECC2949PG35B	170,25 MHz	449,25 MHz	013	018	030	130	001	002	008	142
Alps TEDE9X226A	142,25 MHz	425,25 MHz	011	082	029	002	001	002	008	142
Alps TEDE9-004A	149,25 MHz	424,25 MHz	011	194	028	242	001	002	008	142
Samsung TECC2949PG40B	142,25 MHz	425,25 MHz	011	082	029	002	001	002	008	142
Samsung TECC2949PS40B	142,25 MHz	425,25 MHz	011	082	029	002	001	002	008	142

Explanations	
B1H	High byte of VHF1-VHF3 cross-over frequency
B1L	Low byte of VHF1-VHF3 cross-over frequency
B2H	High byte of VHF3-UHF cross-over frequency
B2L	Low byte of VHF3-UHF cross-over frequency
BS1	Band switching byte for VHF1
BS2	Band switching byte for VHF3
BS3	Band switching byte for UHF
CB	Control byte

According to Reference Divider 62.5 Khz apply the following formula

Value = (Frequency (Mhz) * 1000) / (62.5) + 622 ;
Binary_value (2 bytes) = ToBinary(value);
x can be 1 or 2
Bx-H = MSByte(Binary_value); (most significant byte)
Bx-L = LSByte(Binary_value); (least significant byte)