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Colour TV
Service Manual

Model: 14PHS3/ANZ
Chassis: UOC-TDA9381

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SPECIFICATION

Rated Voltage		AC 110V~250V 50Hz/60Hz	
Power Consumption		65W	
Sound output:		3W×2	
Screen size		Picture tube 21 inch	
System:	Color	RF	PAL SECAM
		AV	NTSC
	Sound	D.K / B.G	
Channel coverage:		VHF Low channel (VL)	=48.25 to 147.25 MHz
		VHF high channel (VH)	=154.25 to 463.25 MHz
		UHF channel (U)	=471.25 to 863.25 MHz
IF		38MHz	
External input/output		Video/Audio (L/R) 1set input at side	
		YUV & SVHS at rear	
		AV output at rear	

- I^2C Bus Control
- Auto Search
- Off/On Timer
- Teletext

THE SURVEY

Table 1, the main IC and functions

Number	Function	IC	Remark
1	Power supply	KA5Q0765RT	N501
2	CPU + SIGNAL PROCESSER	TDA9381	N301
3	Field driver	LA78040 STV9302A	N401
4	Sound processor	TDA9859	N122
5	Sound driver	AN7522N(stereo)	N161
6	AV SWITCH	**TC4052BP**	**N801 (Video)**
7	5V Regulator	L7805CV	N505
8	8V Regulator	L7808CV	N503
9	Memory	AT24C08	N702
10	Photo-coupler	HS817B	N504
11	IR-receiver	HS0038A	U701

THE MAIN CHIPS INSTRUCTION

The UOC ("Ultimate One Chip") TDA9381/61 is adopted in this chassis. This IC is the first available component that contains the complete control and small signal functionality needed for a TV application in one device.

1. The UOC TDA9361/81 pins function description:（ total 64 pins）

Pin1:	Standby control,"1" is on,"0"is off.
Pin2:	SCL.
Pin3:	SDA.
Pin4:	Tuning PWM output.
Pin5:	NTSC SWITCH.
Pin6:	Key board input.
Pin7:	VOL1, controls the 9 pin of the N101 and supplies DC voltage.
Pin8:	Mute control,"1" is mute,"0"is off.
Pin9, Pin12,Pin18, Pin30, Pin35, Pin41, Pin55:	GND.
Pin10 & Pin11:	Band control of the tuner, the two pins needs the pull-up resistance.
Pin13:	SECAM PLL, connected with a capacitor.
Pin14:	+8V power source supply.
Pin15:	Using a capacitor of 220n in series to GND, This pin decouples the internal digital supply voltage of the video processor and minimizes the disturbance to the sensitive analogue parts.
Pin16:	PHI-2 control loop, this pin requires a capacitor at 2.2nF (C) in series to GND.
Pin17:	PHI-1 control loop, the loop filter connected to pin 17 is suitable for various signal conditions like strong/weak and VCR signal. This is achieved by switching of the loop filter time constant by changing the PHI-1 output current.
Pin18:	GND
Pin19:	Bandgap decoupling, the bandgap circuit provides a very stable and temperature independent reference voltage. This reference voltage (4.0 V) ensures optimal performance of the analogue video processor part of the TDA9381 and is used in almost all functional circuit blocks.
Pin20:	AVL filter, according to the different soft edition.
Pin21, Pin22:	Vertical drive output.
Pin23, Pin24:	IF input.
Pin25:	Reference current, This pin requires a resistor to ground. The optimal reference current is 100mA which is determined by this resistor. The 100mA reference current should not be changed because the geometry processor is optimized for this current. Furthermore the output current of vertical drive and EW are proportional to this current.
Pin26:	Vertical saw tooth, This pin requires a capacitor to ground of 100nF.
Pin27:	AGC output. This output is used to control (reduce) the tuner gain for strong RF signals.
Pin28:	Audio de-emphasis.
Pin29:	Sound decoupling. This pin requires a capacitor connected to ground. The pin acts as a low pass filter needed for the DC feedback loop.

Pin30:	GND.
Pin31:	Sound loop filter.
Pin32:	AVL filter, according to the different soft edition.
Pin33:	Horizontal drive signal output, needs a resistance in series to +8V.
Pin34:	Sandcastle output/flyback input.
Pin35:	External audio input, this pin is no use.
Pin36:	EHT tracking/ over voltage protection. If something is wrong, the anode high voltage rises, the heater voltage will rise too. When the rising voltage arrive some limit, the V406 works, the voltage of pin 36 will exceed 3.9V, the TDA9381 will stop working.
Pin37:	PLL loop filter.
Pin38:	CVBS output. Monitor or RF videos can be selected.
Pin39:	+8V supply source.
Pin40:	CVBS input
Pin42:	Y signal input.
Pin43:	C signal input.
Pin44:	Main audio output, this pin is connected to the TDA9859.
Pin45:	**YUV signal input control voltage, 0 = Pin 45 low (< 0.4V), no insertion, 1 = Pin 45 above insertion level (>0.9V), YUVIN inserted.**
Pin46, Pin47, Pin48:	YUV signal input.
Pin49:	ABL. It means beam current limiter input. The R462 & R463 are the control resistances.
Pin50:	Black current input from the CRT board.
Pin51, Pin52, Pin53:	RGB drive signal output to the CRT board.
Pin54:	+3.3V.
Pin55:	GND.
Pin56:	+3.3V.
Pin57, Pin58, Pin59:	12MHz crystal.
Pin60:	Reset, NC in this chassis.
Pin61:	+3.3V
Pin62 & Pin63:	The AV control pins.
Pin64:	IR signal input.

2. Memory AT24C08 is an E^2PROM of 8k, pins describe as follows:

Pin1, Pin2, Pin3, Pin4, Pin7:	GND.
Pin8:	+5V-1 supply.
Pin5:	SDA.
Pin6:	SCL.

SIGNAL PROCESS

The main chip is N301 TDA9381, AV control switch HEF4052 (video), sound process chip is TDA9859 (AV audio), sound driver is N601 AN7522N.

The TV signal inputs into the tuner (A201) from CABLE or antenna. The pin 10 and pin 11 of the N301 are combined to select the band. The pin 4 of the N301 outputs the PWM tuning signal. The IF video signal comes from the IF pin of the tuner. The 38MHz IF signal is coupled to the V308 (pre-amplify) and then to SAWF (Z301). After processed in the SAWF, the 38MHz signal gets to the pin 23 and pin 24 of TDA9381. The IF circuit in TDA9381 includes such unit as the AGC amplifying circuit, 38MHz oscillator, PLL video demodulator, video amplifier, IF identify circuit and AFT circuit. The demodulated signal (CVBS) comes from the pin 38 of TDA9381, the sound signal comes from the pin 44.

The internal CVBS signal needs norm identification then outputs from the pin 38 of TDA9381, via the trap-wave circuit (composed of the V351, Z351, Z352 and so on) feeds back to the pin 40 of TDA9381. The RGB signal comes from the pin51, Pin52, Pin53 of TDA9381, and outputs to the CRT board.

The V911, V921 and V931 are the R、G、B drive transistors. The V912, V913, V922, V923, V932, V933 are the auto low bright balance level output circuit, and generate the low bright level current into the pin 50 of TDA9381.

The internal sound signal comes from the pin 44 of TDA9381, via the coupling capacitor C367 connects to the pin 3 and 5 of TDA9859. The TDA9859 is the audio effect processor, the AN7522N is the driver. The TDA9859 includes bass, treble, balance, surround, effect shortcut options, additional the audio input switch.

THE HORIZONTAL AND VERTICAL CIRCUIT

Through Synchronous separating circuit, the video signal is divided into horizontal-Synchronizing signal and Vertical-Synchronizing signal. The horizontal-Sync pulse coming from the pin 33 is transferred to the horizontal-drive transistor, and will be used to drive the horizontal-transformer. The horizontal-switch transistor is V451, it and the +B supply drives the flyback transformer to generate the anode high voltage, the focus voltage, the screen voltage, the CRT board drive voltage 190V, the vertical drive voltage 15V and -15V.

The vertical sawtooth wave is generated on the pin 21 and 22, and then enters the vertical output amplifier circuit. The vertical output amplifier circuit is realized with the power amplifier IC – LA78040 or STV9302A.

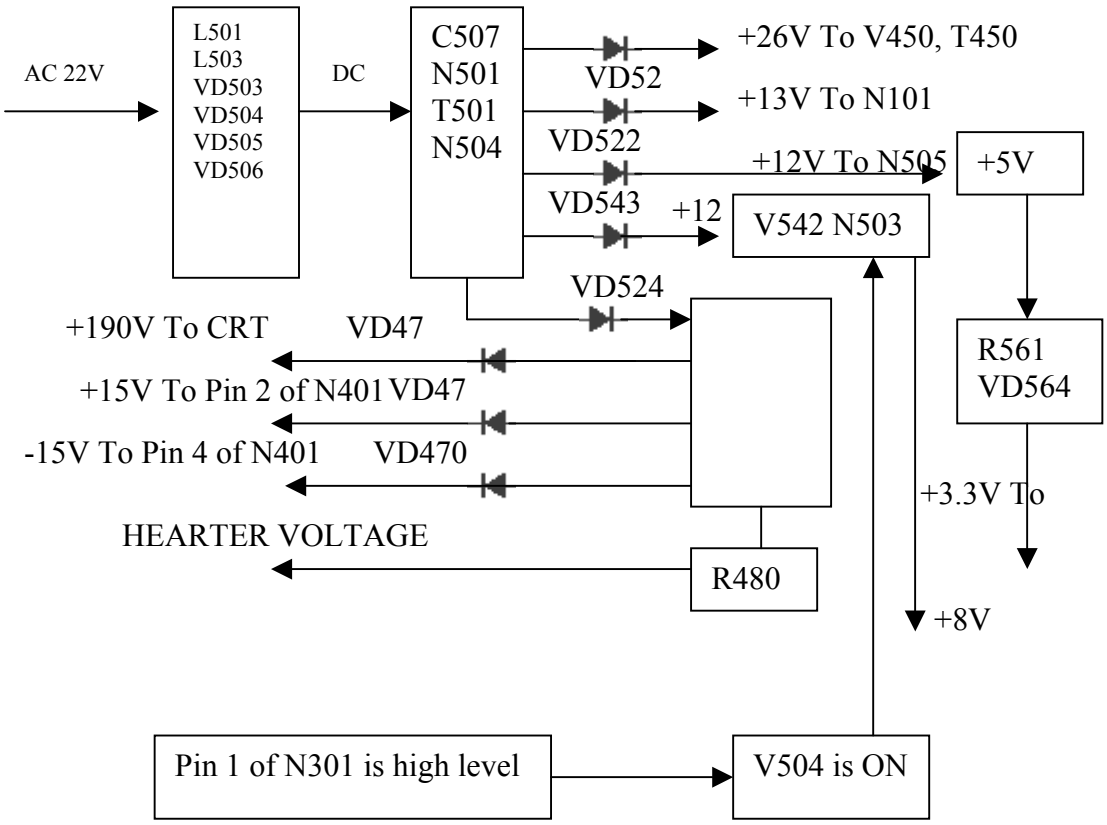
The STV9302A is a 7 pins vertical deflection circuit (3 Amperes) for DC-coupled 90° deflection systems with frame frequencies of 50 or 60 Hz. Two single supply voltages for the scan and two supplies for the flyback are needed.

The vertical drive currents of TDA9381 pins 21 and 22 are connected to input pins 1 and 7 of the STV9302A. Pin 2 is the +15V DC power supply voltage, Pin 4 is the -15V DC power supply voltage. The outputs (pin5) is connected to the series connection of the vertical deflection coil and feedback resistor R406. The voltage across R406 is fed via pin 1 to obtain a deflection current which is proportional to the drive voltage.

Power supply

The IC of KA5Q0765RT is adapted in this chassis; it is the product of Fairchild. It supplies four DC voltages, one is the +B═110V, another is Hcc═26V, the third is 13V (the sound drive voltage), the fourth is +16V. The +16V can generate the +8V. The fifth is +12V, it generate the +5V and +3.3V by the special generators.

Fig.1 The power supplies illustration



FACTORY MENU

Factory menu	Items	Variable	Preset data	Remark
M0	AVL	ON/OFF	ON	Unadjustable
M0	FSL	ON/OFF	OFF	Unadjustable
M0	FMWS	ON/OFF	ON	Unadjustable
M0	FFI	ON/OFF	OFF	Unadjustable
M0	OSO	ON/OFF	ON	Unadjustable
M0	FCO	ON/OFF	OFF	Unadjustable
M0	WOOFER	ON/OFF	OFF	Unadjustable
M0	DUAL OUT	0~1	0	Unadjustable
M0	Volume mode	0~1	1	Unadjustable
M0	Vol pin	Push-pull open-drain	Push-pull	Unadjustable
M1	BAND	0~2	2	Unadjustable
M1	AV CFG	0~9	3	Unadjustable
M1	NTSC MX	USA JAP	USA	Unadjustable
M1	VIDEO OUT	IF CVBS	CVBS	Unadjustable
M1	PIN5	NTSC RGB	RGB	Unadjustable
M1	PRO	0~3	0	Unadjustable
M2	VISION IF	38 38.9M	38M	Unadjustable
M2	DK	ON/OFF	ON	Unadjustable
M2	BG	ON/OFF	ON	Unadjustable
M2	I	ON/OFF	OFF	Unadjustable
M2	M	ON/OFF	OFF	Unadjustable
M2	SIF PREFER	BG DK I M	DK	Unadjustable
M2	AUTO SOUND	ON/OFF	ON	Unadjustable
M3	START	ON/OFF	ON	Unadjustable
M3	ENGLISH	ON/OFF	ON	Unadjustable
M3	ARABIC	ON/OFF	ON	Unadjustable
M3	PERSIAN	ON/OFF	ON	Unadjustable
M3	TURKISH	ON/OFF	ON	Unadjustable
M3	FRANCE	ON/OFF	ON	Unadjustable
M3	RUSSIA	ON/OFF	ON	Unadjustable

Factory menu	Items	Variable	Preset data	Remark
M4	SUBCON	0~63	45	Adjustable
M4	SUBCOL	0~63	63	Adjustable
M4	SUBSHP	0~63	36	Adjustable
M4	SUBTINT	0~63	28	Adjustable
M4	YDLY PAL	0~15	7	Adjustable
M4	YDLY NTSC	0~15	7	Adjustable
M4	YDLY SEC	0~15	7	Adjustable
M4	YDLY AV	0~15	7	Adjustable
M4	UOC VOL	ON/OFF	OFF	Adjustable
M4	UOC VOL	0~63	45	Adjustable
M4	CATHODE	0~15	7	Adjustable
M5	OSD VPOS	0~63	53	Adjustable
M5	OSD HPOS	0~48	9	Adjustable
M5	WIDE	0~63	2	Adjustable
M5	ZOOM	0~63	53	Adjustable
M5	NENU TITLE	0~6	3	Unadjustable
M5	LOGO ADDRESS	0~33	0	Unadjustable
M5	LOGO VALUE	0~95	0	Unadjustable
M5	LOGO WRITE	***	***	Unadjustable
M6	SHIPMODE			Unadjustable
M6	SEARCH SPEED	0~3	0	Adjustable
M7	AGC-TOP	0~63	28	Adjustable
M7	AGC-SPEED	0~3	2	Unadjustable

Factory menu	Items	Variable	Preset data	Remark
M8	FREQUENCY	50 60HZ	50HZ	Adjustable
M8	VSLOPE	0~63	30	Adjustable
M8	VSHIFT	0~63	36	Adjustable
M8	VAMP	0~63	28	Adjustable
M8	VSCOR	0~63	31	Adjustable
M8	HSHIFT	0~63	31	Adjustable
M8	RGB HSHIFT	0~63	31	Adjustable
M8	RGB POS	0~48	31	Adjustable
M9	BT	0~63	45	Adjustable
M9	CT	0~63	48	Adjustable
M9	SC	ON/OFF	OFF	Adjustable
M9	RB	0~63	32	Adjustable
M9	GB	0~63	32	Adjustable
M9	RD	0~63	32	Adjustable
M9	GD	0~63	32	Adjustable
M9	BD	0~63	32	Adjustable
M9	SB	0~63	40	Unadjustable

M entrance process:
First press the menu, when the picture (bright and contrast) OSD reveals, then press 8500.

APPENDIX

HEF4052B illustration

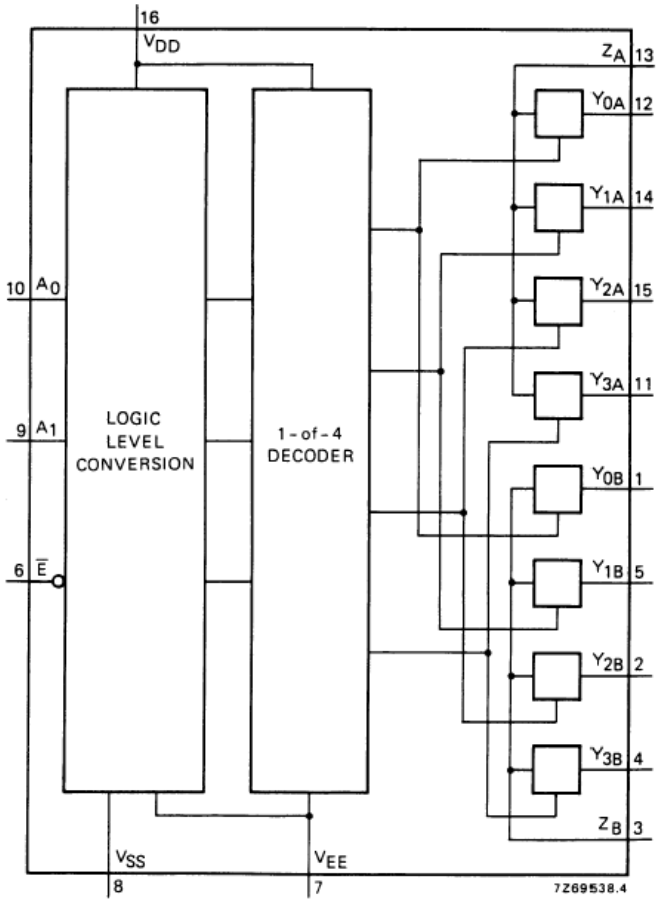


Fig.1 Functional diagram.

PINNING

Y_{0A} to Y_{3A}	independent inputs/outputs
Y_{0B} to Y_{3B}	independent inputs/outputs
A_0, A_1	address inputs
$\overline{E}$	enable input (active LOW)
Z_A, Z_B	common inputs/outputs

FAMILY DATA,
I_{DD} LIMITS category MSI

See Family Specifications



Fig.2 Pinning diagram.

HEF4052BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4052BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4052BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

TDA9859 illustration 1

PINNING

SYMBOL	PIN	DESCRIPTION
$SCIN_L$	1	SCART input; left channel
P1	2	port 1 output
MIN_L	3	MAIN input; left channel
C_{SMO}	4	smoothing capacitor of reference voltage
MIN_R	5	MAIN input; right channel
V_P	6	supply voltage
$SCOUT_R$	7	SCART output; right channel
GND	8	ground
$MOUT_R$	9	MAIN output; right channel
LIN_R	10	input to right loudspeaker channel
C_{BR1}	11	bass capacitor connection 1; right channel
C_{BR2}	12	bass capacitor connection 2; right channel
n.c.	13	not connected
C_{TR}	14	treble capacitor connection; right channel
$LOUT_R$	15	loudspeaker output; right channel
SCL	16	serial clock input; I^2C-bus
SDA	17	serial data input/output; I^2C-bus
$LOUT_L$	18	loudspeaker output; left channel
C_{TL}	19	treble capacitor connection; left channel
n.c.	20	not connected
C_{BL2}	21	bass capacitor connection 2; left channel
C_{BL1}	22	bass capacitor connection 1; left channel
LIN_L	23	input to left loudspeaker channel
$MOUT_L$	24	MAIN output; left channel
MAD	25	module address select input
$SCOUT_L$	26	SCART output; left channel
C_{PS2}	27	pseudo stereo capacitor 2
AIN_L	28	AUX input; left channel
C_{PS1}	29	pseudo stereo capacitor 1
AIN_R	30	AUX input; right channel
P2	31	port 2 output
$SCIN_R$	32	SCART input signal RIGHT

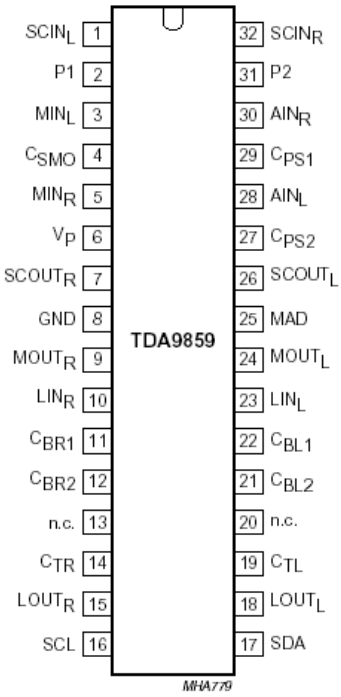
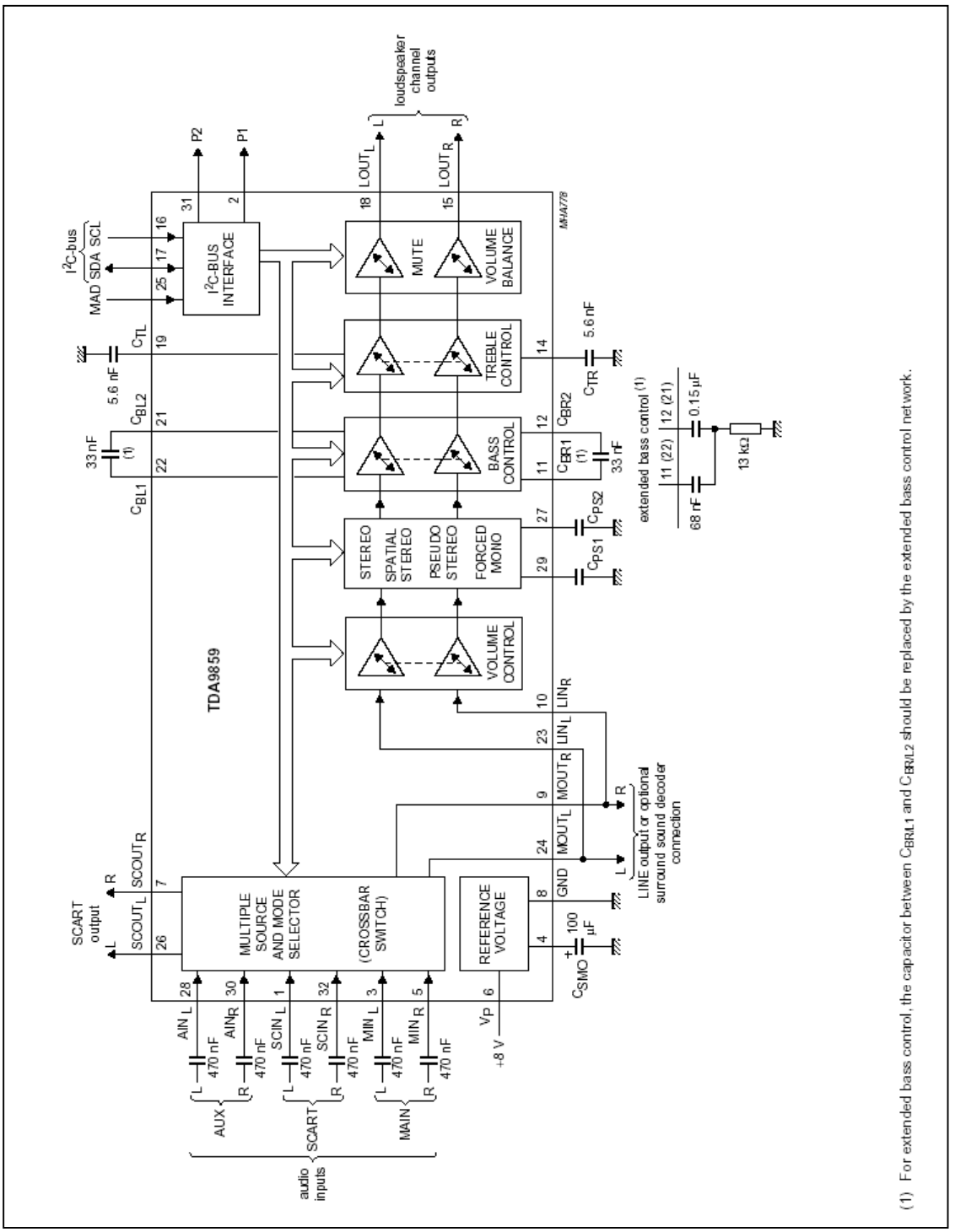
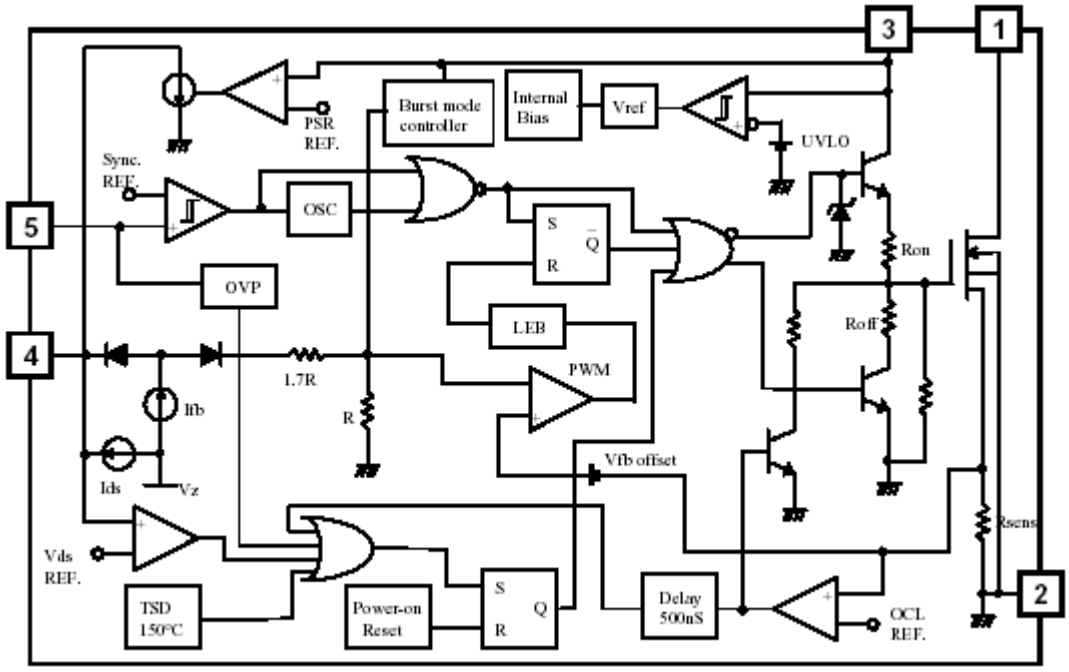


Fig.2 Pin configuration.

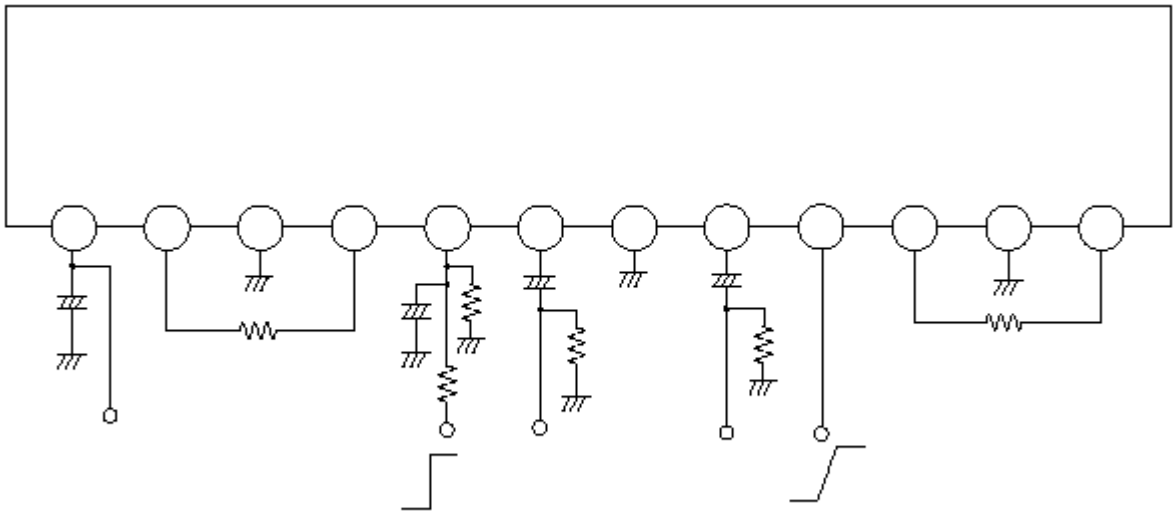
TDA9859 illustration 2



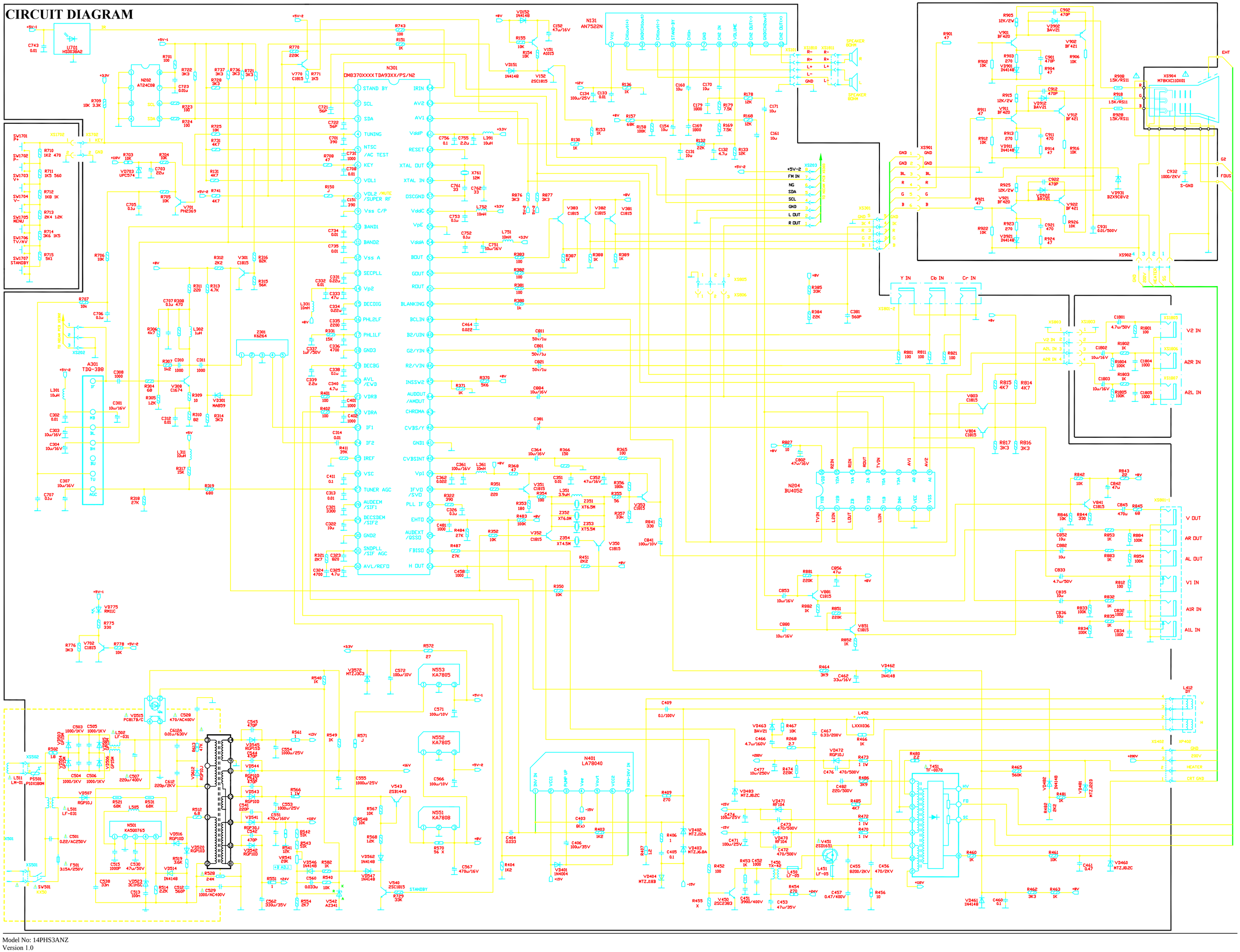
KA5Q0765RT illustration



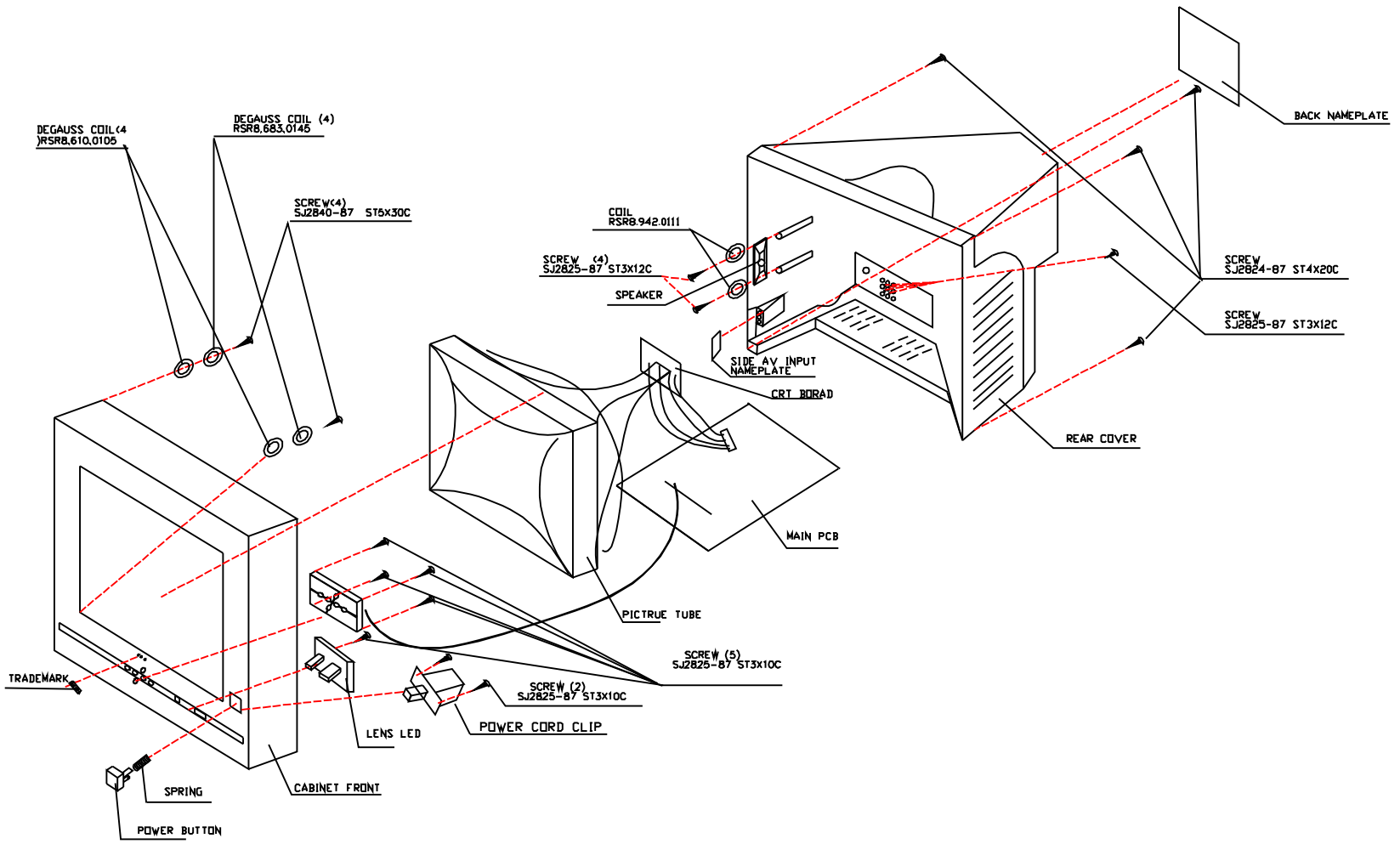
AN7522N illustration



CIRCUIT DIAGRAM



EXPLODED VIEW WITH PART NAME



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