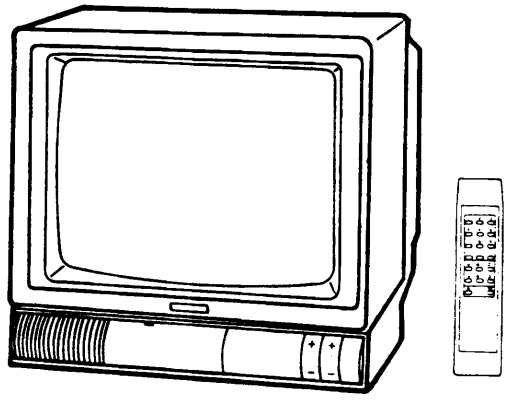
COLOUR TELEVISION SERVICE MANUAL

CHASSIS NO. C-43
PAL SYSTEM



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SPECIFICATIONS

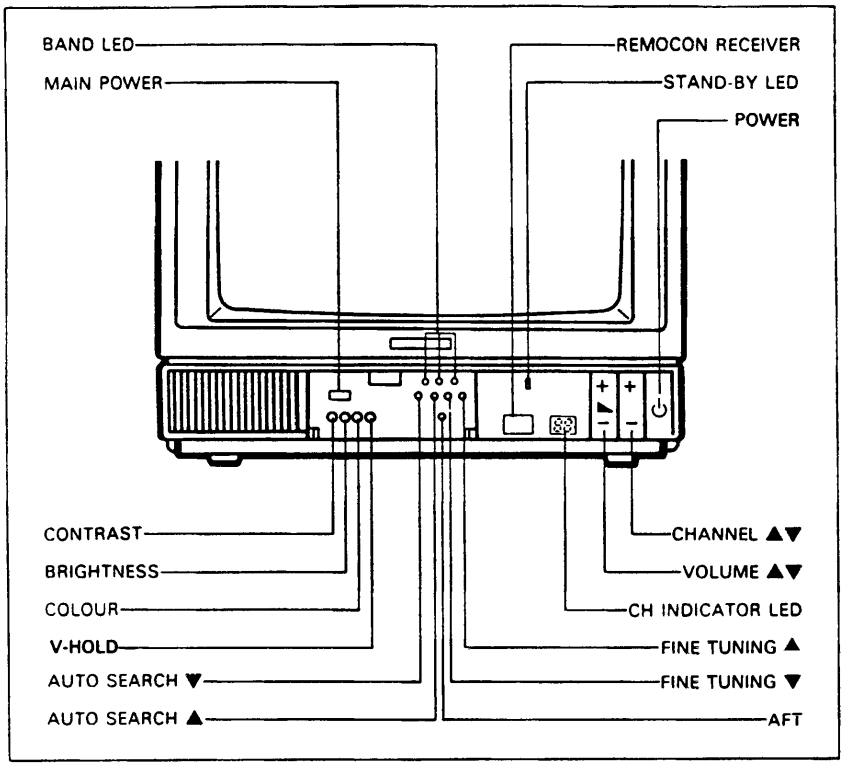
Power Input	AC 240V, 50Hz
Power Rating	(14") 67 Watts, (20") 74 Watts
Tuning Method	Voltage Synthesizer Tuning System
Television System	PAL I
Receiving Channels	VHF Channels: 21 to 69
Antenna Terminal	75 Ohm Unbalanced Type for UHF
Picture IF Carrier Frequency	39.5 MHz
Sound IF Carrier Frequency	33.5 MHz
Color Sub-Carrier Frequency	35.07 MHz
Sound Output	1.0 Watts (at 10% THD)
Speaker	5 Watts 8 Ohm
Picture Tube	(14") A34JLL70×01 (20") A48JLL70×02
Dimensions	(14") W×H×D=368×341×372 (20") W×H×D=498×458×478

WARNING

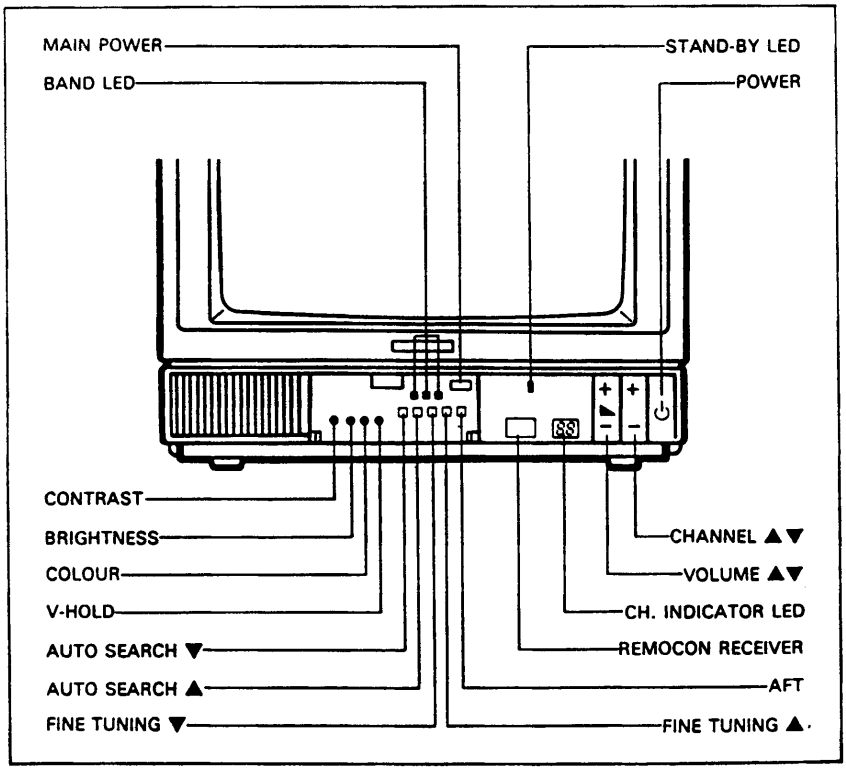
The chassis in this receiver is hot. Use an isolation transformer between the fine cord plug and power receptacle, when servicing this chassis.
To prevent electric shock, do not remove cover. No user-serviceable parts inside. Refer servicing to qualified service personnel.

LOCATION OF CONTROL

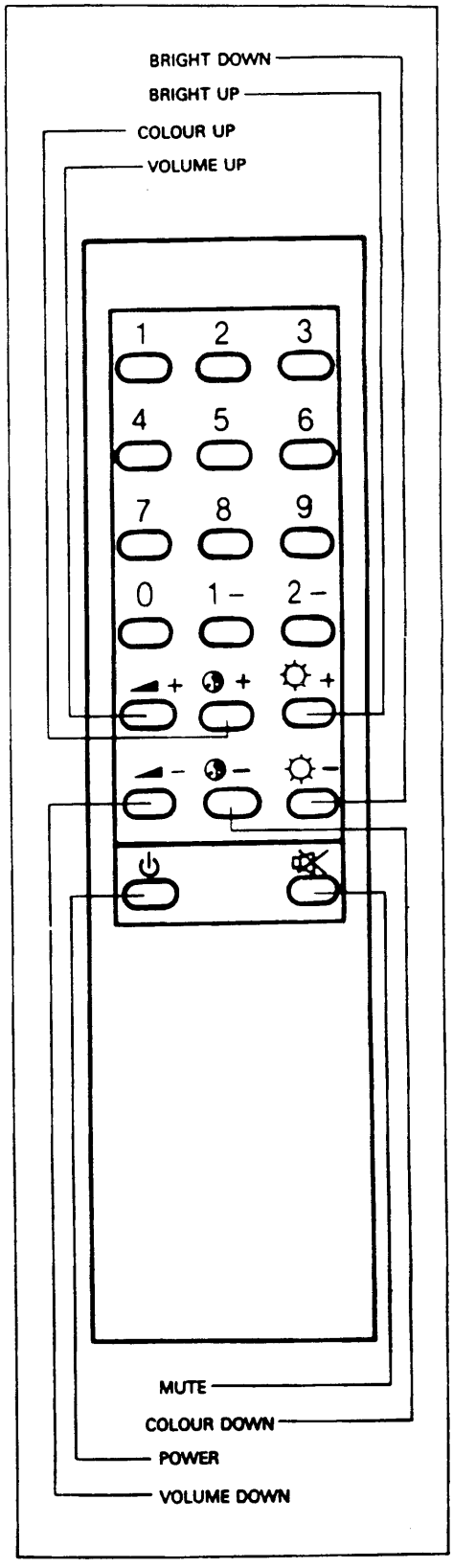
• 14 INCH FRONT PANEL



• 20 INCH FRONT PANEL



• REMOTE CONTROL UNIT



INSTALLATION AND SERVICE ADJUSTMENTS

WARNING: BEFORE SERVICING THIS CHASSIS, READ THE "X-RAY RADIATION PRECAUTION", "SAFETY PRECAUTION" AND "PRODUCT SAFETY NOTICE" ON PAGE 2 OF THIS MANUAL.

GENERAL INFORMATIONS

All adjustments are thoroughly checked and corrected when the receiver leaves the factory. Therefore the receiver should operate normally and leaves the factory. Therefore the receiver should operate normally and produce proper colour and B/W picture upon installation. However, several minor adjustments may be required depending on the particular location in which the receiver is operated.

This receiver is shipped completely in cardboard carton. Carefully draw out the receiver from the carton and remove all packing materials.

Plus the power cord into a convenient 240 volts 50Hz AC two pin power outlet or frequency.

Turn the receiver ON and adjust the FINE TUNING for best picture detail.

Check and adjust all the customer controls such as BRIGHTNESS, CONTRAST and COLOUR Controls to obtain natural colour or B/W picture.

AUTOMATIC DEGAUSSING

A degaussing coil is mounted around the picture tube so that external degaussing after moving the receiver is normally unnecessary, providing the receiver is properly degaussed upon installation. The degaussing coil operates for about 1 second after the receiver is switched ON. If the set is moved or faced in different direction, the power switch must be switched off at least 10 minutes in order that the automatic degaussing circuit operates

VERTICAL OSCILLATOR ADJUSTMENT

HEIGHT Control (R352) on MAIN Board changes the size of the picture or pattern, having an equal effect on the top and bottom. Make final adjustment to overscan the mask 2cm at top and bottom.

FOCUS ADJUSTMENT

Adjust FOCUS Control on FOCUS PACK for well defined scanning lines in the centre area on the screen.

DELAYED R-F AGC ADJUSTMENT

1. Tune the set in the strongest station in your area.
2. Turn AGC DELAY CONTROL (R152) on MAIN Board to fully clockwise position.
3. Adjust AGC DELAY Control counter-clockwise until noise (snow) disappears on the screen.

AFT (Automatic Fine Tuning) FIELD ALIGNMENT

1. Tune the set to an active channel and adjust fine tuning for best picture.
2. Press and release AFT button, and adjust Coil (T102) on MAIN Board for best picture. Picture quality should be the same as that obtained in Step 1.
3. Check the AFT action by using the fine tuning up/down button and AFT button.

SIF DET. ADJUSTMENT (L651: SIF DET. COIL)

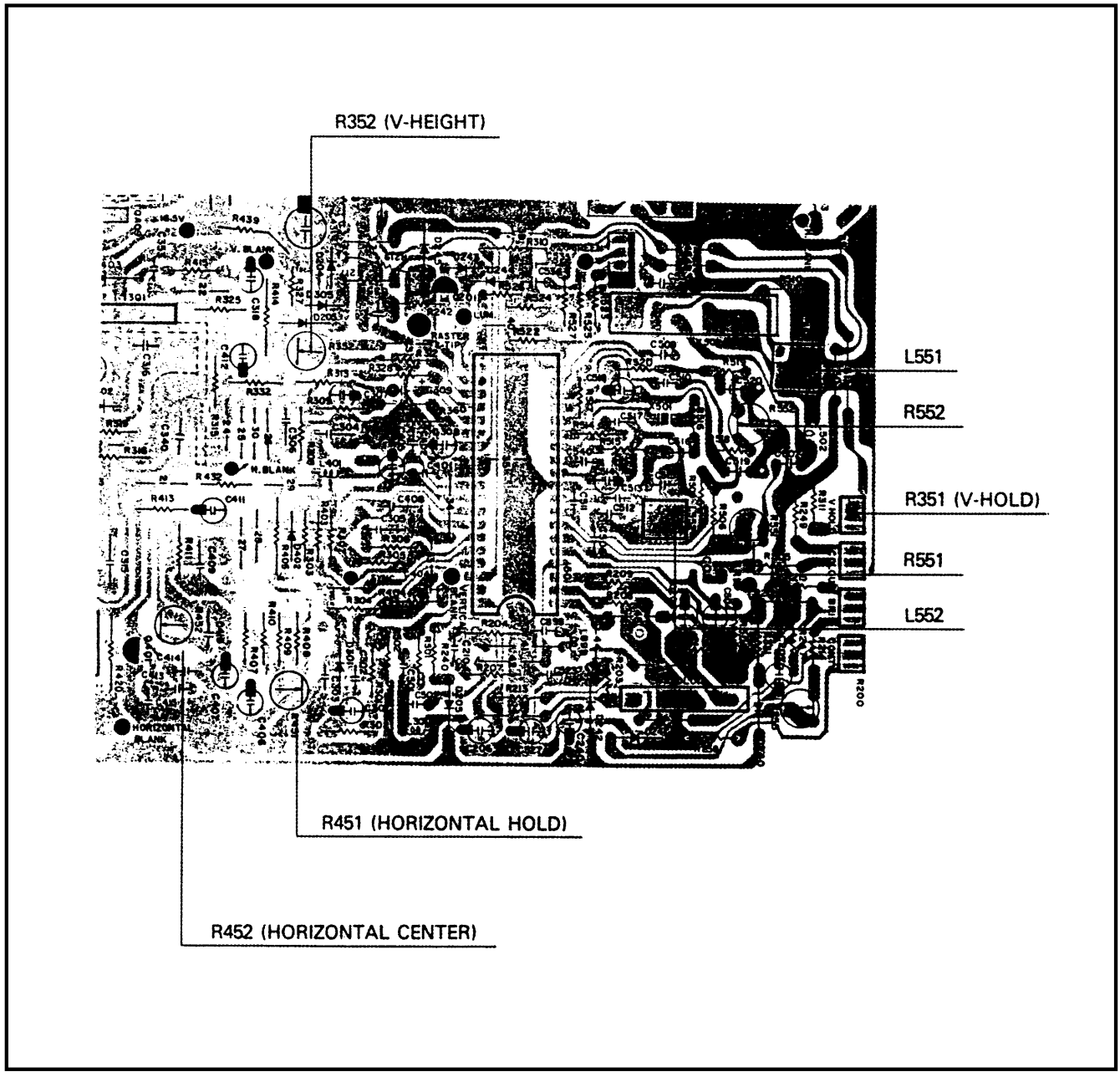
1. Tuen in programme which has a pure tone (For example, 400Hz or 1kHz) with SIF carrier.
2. Adjust SIF DET. coil L651 so that the sound output power goes to the maximum.

WHITE BALANCE ADJUSTMENT

The purpose of this procedure is to optimize the picture tube to obtain good black and white picture at all brightness levels while at the same time achieving maximum usable brightness. Normal RF AGC setting and purity adjustment must proceed this procedure.

Set the CONTRAST control to maximum and the BRIGHTNESS control to maximum and the SHARPNESS control to the center position.

1. Tune in a monochrome channel and warm up the set for 15 minutes.
2. Set the R.G.B. bias controls (R554, R559, R564) to minimum.
3. Set the G.B drive controls (R560, R565) to the center position.
4. Rotate the screen control fully counter clockwise.
5. Disconnect the luminance output terminal connector (Raster tip) and connect TP S to ground with a jumper wire.
6. Rotate the screen control gradually clockwise until the first horizontal line appears on the screen.
7. If the first horizontal line is red, adjust R559 and R564 to increase the green and blue component level to get a white horizontal line.
8. Remove the jumper wire and connect back the luminance output terminal (Raster tip). Set the BRIGHTNESS and CONTRAST controls at normal position. Adjust R560, R565 to maintain a good white balance at the brightest part of the screen.
9. Turn the BRIGNTNESS and CONTRAST controls to maximum and minimum. Observe the screen white balance, if it is not proper in high brightness or low brighness condition, adjust R.G.B bias controls or G.B drive controls respecitively in order to maintain a good white balance in both low and high luminance conditions.



CONVERGENCE ADJUSTMENTS

Note: Before attempting any convergence adjustments, the receiver should be operated at least fifteen minutes.

■ Center Convergence Adjustment

1. Receive crosshatch pattern with a colour bar signal generator.
2. Adjust the BRIGHTNESS and CONTRAST Controls for well defined pattern.
3. Adjust two tabs of the 4-Pole Megnets to change the angles between them (See Fig. 2) and superimpose red and blue vertical lines in the Center area of the picture screen. (See Fig. 3)
4. Turn the both tabs at the same time keeping the constant angle to superimpose red and blue horizontal lines at the center of the screen. (See Fig. 3)
5. Adjust two tabs of 6-Pole Magnets to superimpose red/blue line and green one. Adjusting the angle affects the vertical lines and rotating both magnets affects the horizontal lines.
6. Repeat adjustments 3, 4, 5 with understanding red, green and blue moverment, because 4-Pole Magnets and 6-Pole Magnets have mutual affection and it makes dots movement complex.

■ Circumference Convergence Adjustment

1. Loosen the clamping screw of deflection yoke to allow the yoke to-tilt.
2. Put a wedge as shown in Fig. 1 temporarily. (Do not remove cover paper on adhesive part of the wedge.)
3. Tilt front of the deflection yoke up or down to obtain better convergence in circumstance. (See Fig. 3) Push the yoke to fix the yoke temporarily.
4. Put other wedge into bottom space and remove the cover paper to stick.
5. Tilt front of the yoke right or left to obtain better convergence in circumstance. (See Fig. 3)
6. Keep the yoke position and put another wedge in either upper space. Remove cover paper and stick the wedge on picture tube to fix the yoke.
7. Detach the temporarily mounted wedge and put it in another upper space. Stick it on picture tube to fix the yoke.
8. After fixing three wedges, recheck overall convergence. Tighten the screw firmly to fix the yoke and check the yoke in firm.
9. Stick 3 adhesive tapes on wedges as shown in Fig. 1.

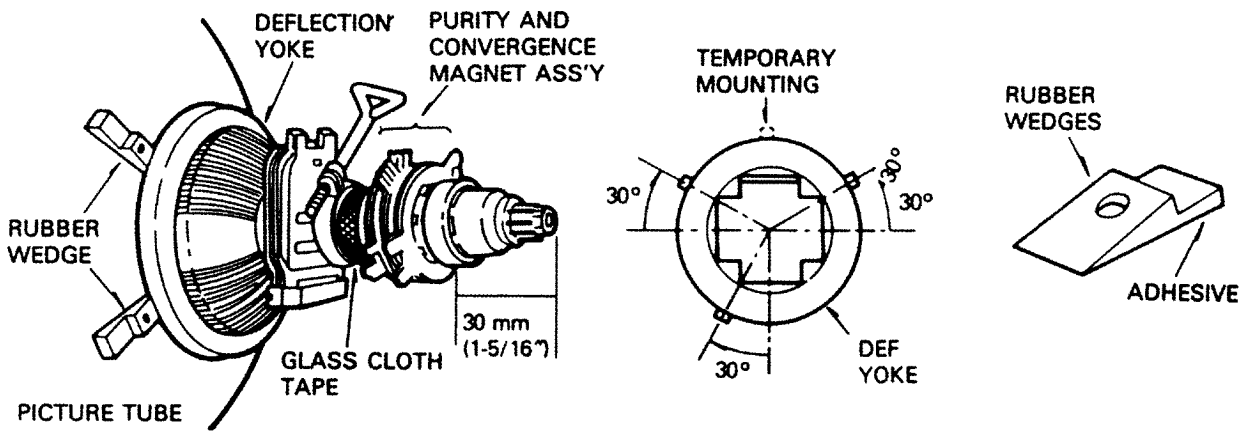
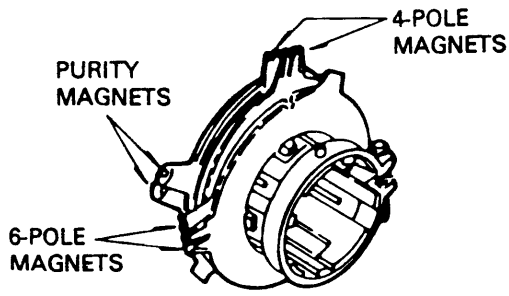
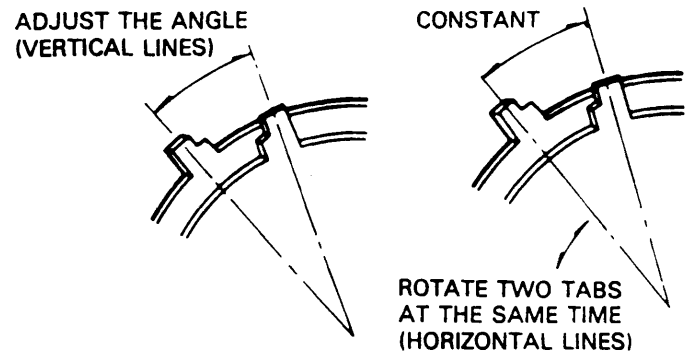


Fig. 1 RUBBER WEDGES LOCATION

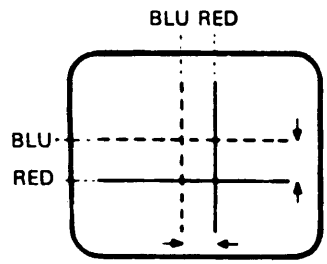


CONVERGENCE MAGNET ASSEMBLY

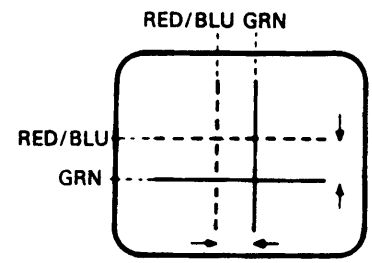


ADJUSTMENT OF MAGNETS

Fig. 2

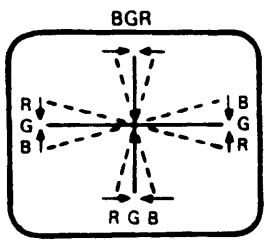


4-POLE MAGNETS MOVEMENT

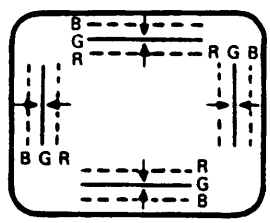


6-POLE MAGNETS MOVEMENT

Center Convergence by Convergence Magnets



INCLINE THE YOKE UP (OR DOWN)



INCLINE THE YOKE RIGHT (OR LEFT)

Circumference Convergence by Deflection Yoke

Fig. 3 Dot Movement Pattern

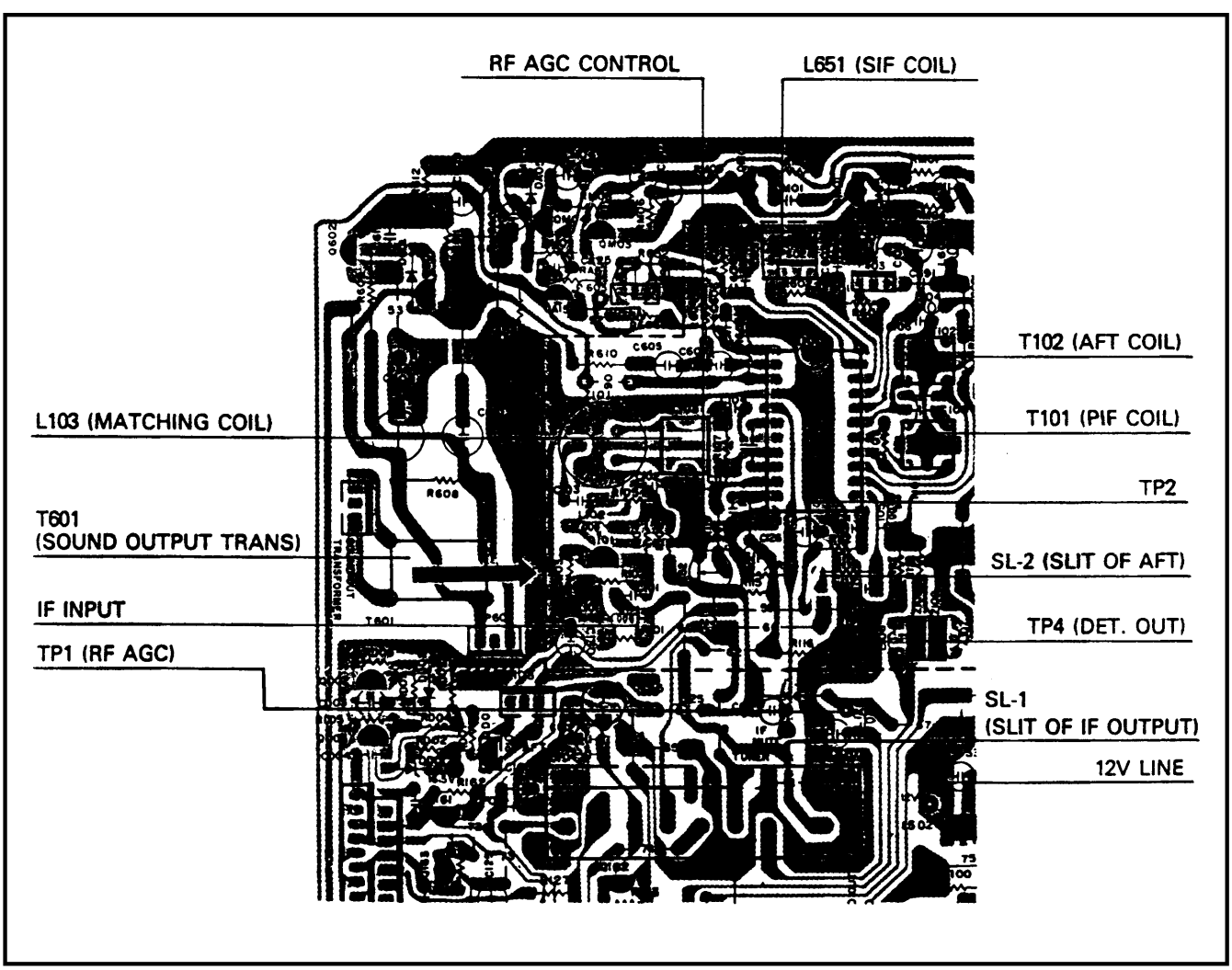
GENERAL ALIGNMENT INSTRUCTIONS

THIS RECEIVER IS TRANSISTORIZED SPECIAL CARE MUST BE TAKEN WHEN SERVICING. READ THE FOLLOWING NOTES BEFORE ATTEMPTING ALIGNMENT.

- Alignment requires an exacting procedure and should be undertaken only when necessary.
- Isolation transformer must be used to prevent shock hazard.
- The test equipment specified or its equivalent is required to perform the alignment properly. Use of equipment which does not meet these requirements may result in improper alignment.
- Correct matching of the equipment is essential. Failure to use proper matching will result in responses which cannot represent the true operation of the receiver.
- Use of excessive signal from a sweep generator can cause overloading of receiver circuit. Overloading should be avoided to obtain a true response curve. Insertion of markers from the marker generator should not cause distortion of hte response.
- The AC Power line voltage should be kept 240 Volts while alignment.
- Do not attempt to connect or disconnect any wire while the receiver is in operation. Make sure the power cord is disconnected before replacing any parts in the receiver.

TEST EQUIPMENTS

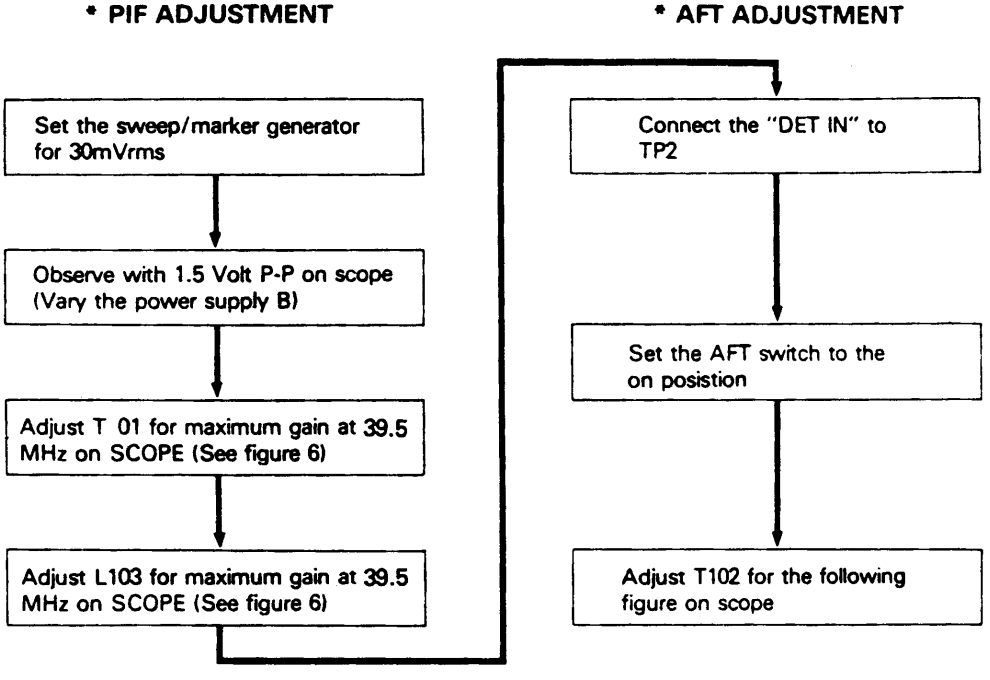
Digital voltmeter	National Model VP-2600A or equivalent.
Oscilloscope	Tektronix Model 2215A or equivalent.
Direct/Low-capacity probe	Tektronix Model P6120 or equivalent. (Accessory of oscilloscope)
Color-Bar/Dot/Crosshatch generator	Tektronix Model 146 or equivalent.
PIF sweep marker generator	Nihon Tsushinki Model 4723 or equivalent.
Power supply	Academy Model 150A or equivalent.
Isolation transformer	Voltage adjustable type having capacity of more thn 150 watts.



■ PICTURE I-F SWEEP ALIGNMENT AND AFT ALIGNMENT

- Refer to Fig. 4, 5 and 6 for alignment points and test equipments connections.

1. Open the SLIT-1 (IF output terminal of TUNER) and SLIT-2 (AFT terminal of TUNER).
2. Connect the "Output Terminal" of the sweep/marker generator to the I-F input on Main Board.
3. Connector the "DET IN" with direct probe to TP4 on the Main Board.
4. Supply + 12 volt bias to 12 volt line and +8 volt bias to terminal "TP1" on Main Board.
5. Set the AGC DELAY Control (R152) on Main Board fully clockwise.
6. Proceed with the alignment steps following the chart below.
7. If the response on oscilloscope appears unstable, disconnect the RF AGC lead temporarily.



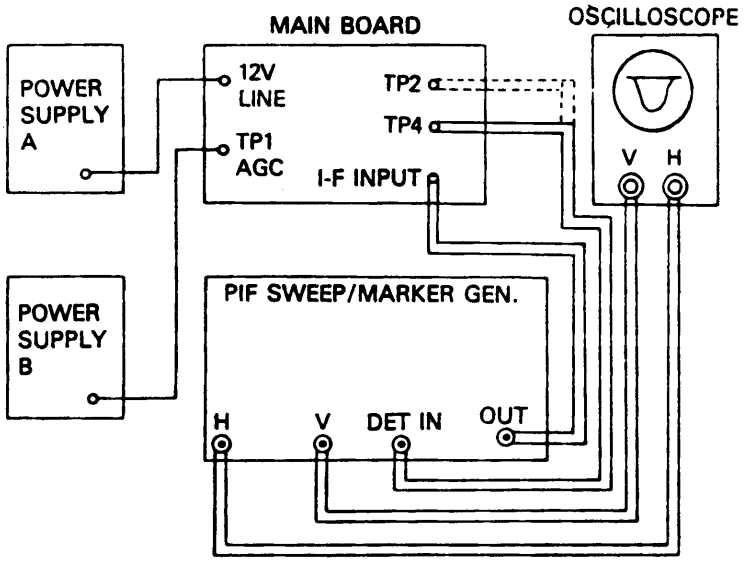


Fig. 4 Picture I-F Sweep Alignment

*** After completing the above steps, disconnect equipment and adjust the AGC circuit.**

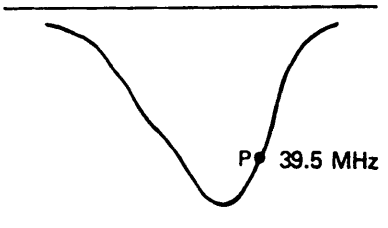


Fig. 5 PIF RESPONSE CURVE

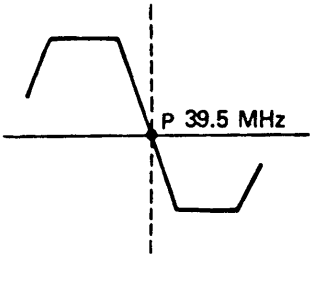


Fig. 6 AFT RESPONSE CURVE

IC OPERATION DESCRIPTION

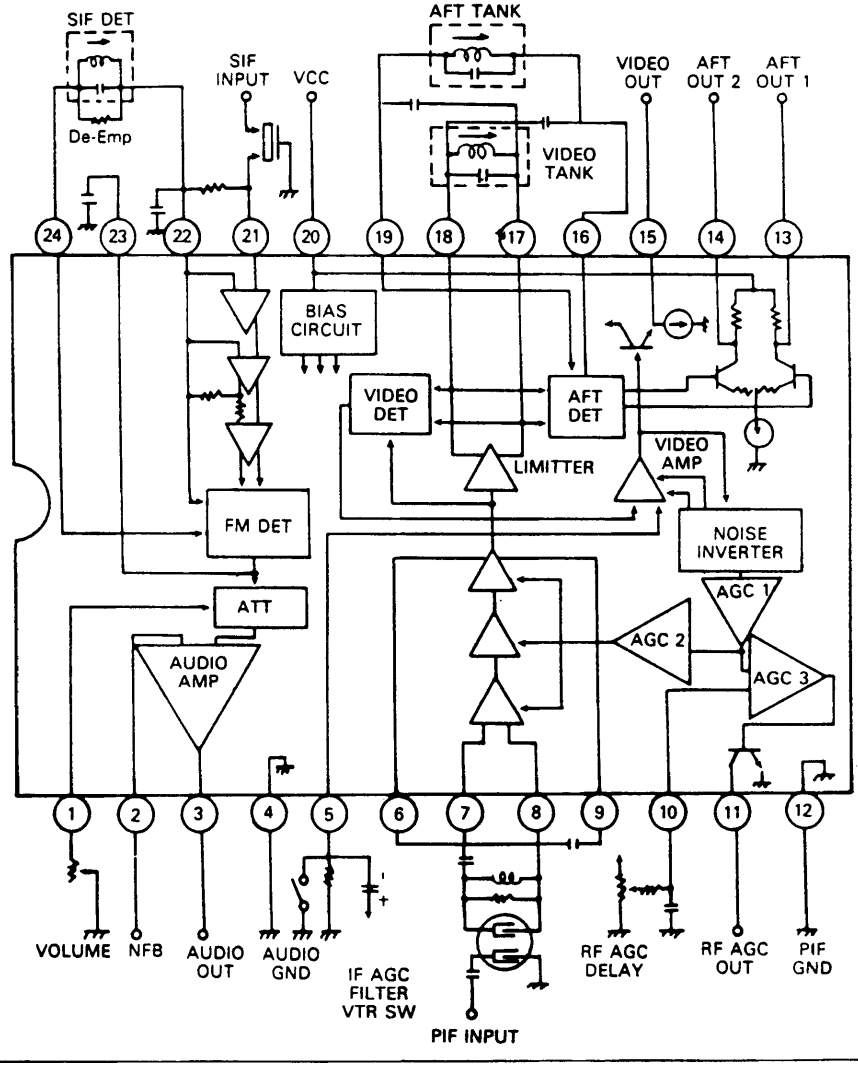
1. TA7680AP/81AP

(1) Functions of the TA7680AP/81AP

The TA7680AP/81AP combines a PIF system and an SIF system in a 24 leads dual-in-line plastic package. The PIF system is equal to the system of the TA7607AP/11AP. And the SIF system is consists of a 3-stage limiter amplifier, a synchronous FM detector, an electronic volume control and an AF pre-amplifier. This device is designed to have wide application capability with minimal external parts and adjustments.

The TA7680AP/81AP realizes a PAL CTV system in conjunction with the TA7698AP video-chroma-deflection, or an NTSC CTV system with the TA7644BP video-chroma-deflection.

BLOCK DIAGRAM



(2) Operation of the PIF section

The PIF section provides all the function which a PIF stage requires. The difference between the TA7680AP and the TA7681AP is only the output polarity of the RF AGC. The TA7680AP has a reverse RF AGC output for a FET top tuner, and the TA7681AP has a forward RF AGC output for a NPN top tuner. These are identical to the TA7607AP and the TA7611AP.

The TA7680AP/81AP realizes a high performance PIF subsystem in conjunction with a suitable SAW (Surface Acoustic Wave) filter, with minimal external components and adjustments.

Followings are the operation description based on the block diagram.

(a) PIF amplifier stage

The PIF amplifier is a 3-stage AGC amplifier. The sensitivity of this stage is 110uVrmsTyp. @58MHz, or 52uVrmsTyp. @45MHz.

Terminal #7 and #8 are the input terminals. A single-ended or a differential input configuration is capable. Terminal #6 and #9 are the decoupling terminals for the internal bias circuit.

The gain of this stage is controled by the internal peak-value AGC circuit. The output of this stage is connected to the video detector stage internally.

(b) Video Detector

The amplified PIF signal is applied to the video detector.

The picture carrier component is derived from the PIF signal, limited and phase shifted by a tank circuit connected to #17 and #18 terminal to produce a switching carrier for the synchronous video detector.

The SIF signal is detected at the same time (Inter carrier Detection).

Detected composite video signal is applied to video output stage, AGC circuit and the noise inverter circuit throgh a part of the video amplifier.

(c) Video Amplifer

The video amplifier consists of a buffer amplifier and an output amplifier which has 6mA output current capability. Therminal #15 is the output terminal for the composite video signal and the SIF signal.

The composite output signal has 2.5V sync-tip level (Sync negative) and $2Vp_{-}p$ amplitude. This output is applied to the video inverter amplifier of the video-chroma-deflection IC, and the DC component of the output signal can be a bias source of the sequential amplifier. The composite video signal is also applied to the AGC circuit and the noise inverter circuit internally.

(d) Noise Inverter

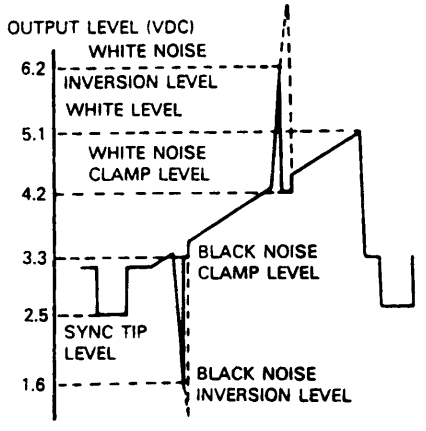
Operation level of the internal IF AGC of the TA7680AP/81AP is determined by the sync-tip level mentioned above. If the composite video signal includes black pulse noises which exceeds 2.5V to the minus side, they may cause mis-operation of the AGC, unstability of the synchronization or degradation of the S/N ratio.

Also white pulse noises cause degradation of the S/N ratio.

The TA7680AP/81AP provides noise inverter circuits for both noises to keep a stable operation. A noise which exceeds the threshold level is inverted to a gray level (clamp level).

The relation of the threshold levels and clamp levels are shown below. This inverter circuit performs excellent capability of noises without any external components or control signals.

Video output level and Noise Inversion levels



(e) AGC Circuit

The composite video signal is also applied to the AGC circuit.

The AGC circuit is consist of the internal IF AGC circuit and the RF AGC circuit with the delay point adjustment circuit.

At the input of the AGC circuit, an 12dB/Oct. L.P.F. is equipted to prevent abnormal AGC operation such as AGC latch up caused by excessive SIF signal component or high frequency noise components.

The internal IF AGC controls the 3-stage PIF amplifier gain.

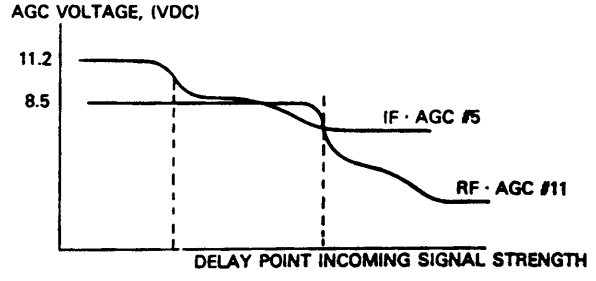
The total gain control range (or the gain reduction range) is 64dB typ..

The AGC response speed is determined by an external CR value connected to the #5 terminal. If the time constant is too small, it will cause the "zag" during vertical sync period. And if too big, the system will not be able to track rapid input signal level changes such as flattering caused by an airplane and so on.

The #11 terminal is an open-collector RF AGC output terminal.

The starting point of the RF AGC (Delay point) is determined by a D.C. voltage of the #10 terminal. The output polarity of the RF AGC and the IF AGC control voltage change by the input signal level are shown bellow. The TA7680AP is the reverse RF AGC type for an FET top tuner, and the TA7681AP is the forward RF AGC type for an NPN top tuner.

TA7680AP
AGC Characteristics



(f) AFT Circuit

A multi-plier type phase detector is applied to the AFT detector.
The reference signal is the input PIF signal (limited picture carrier) and the input signal of the AFT detector is derived from the PIF tank and phase shifted by an AFT tank circuit which is connected between the #16 terminal and the #19 terminal.

To keep stable AFT operation, a cross-coupling connection between the PIF tank and the AFT tank is recommendable. This connection is able to cancel or compensate stray capacitances between PIF tank circuit and AFT tank circuit.

Terminal #13 and #14 are the differential AFT output terminals, which enable wide application capability.

(3) Operation of the SIF Section

The SIF section Provides all the function for an SIF sub-system, which consist of a 3-stage limiter amplifier, synchronous FM detector electionic volume control and audio pre-amplifier with NFB terminal. To complete the whole SIF sub-system, only an power output stage (two small power transistors for the SRPP construction) is required

Followings are the operation discription based on the block diagram.

(a) SIF Limiter Stage

The SIF limiter amplifier concists of 3-stage differential amplifier.
The #21 terminal is the input terminal of the SIF signal, the #22 is by passing and bias terminal for the SIF limiter and FM detector.
The output of the limiter amplifier is applied to the FM detector through balanced emiter-followers.

(b) FM Detector

The FM detector is a double balanced type synchronous detector using the limiter output and phase shifted signal by an SIF DET tank circuit connected between the #24 and #22 terminak As the operation bias of the detector circuit is derived from the limiter stage (#22), the external phase shifter is required DC conduction #22 to #24. A simple Q-damped LC tank circuit is recommendable for the phase shifter. This common bias construction realises "One terminal FM detector circuit".

Operating characteristics of the detector is determined or designed by the external LC tank circuit. The characteristics example is shown bellow.

Detected AF signal is directly connected to the electronic volume control circuit through a level shift circuit.

The #23 terminal is for de-emphasis by connecting a suitable external capacitor (Provided internal resister for the de-emphasis is 15 kohm typ..). This terminal can be used as a fixed level detected output terminal for a MPX stereo application.

(c) Electronic Volume Control

The electronic volume control is the dual-balance type. The simplified circuit construction is shown bellow. The #1 terminal is control terminal. The output level (volume control level) is determined applied voltage of the #1. The control characteristics is also shown bellow. The effective control range is 3V to 6V, and the maximum colume control range is 72dB typ..

(d) Pre-amplifier

The output of the volume control is applied to the inverting input of the NF pre-amplifier. The #2 terminal is non-inverting input and the #3 is the output terminal of the NF amplifier.

The typical open loop gain of this stage is 24dB typ..

The #2 terminal can be used as a direct output terminal of the volume control.

2. TA7698AP

(1) Function of the TA7698AP

The TA7698AP combines a PAL/NTSC Video-Chroma sub system and a Deflection combination on a single chip to provide a PAL or a PAL/NTSC color television.

This device includes a Video amplifier, PAL and NTSC color Demodulators designed to provide color differential outputs, an improved Sync-separator, a Horizontal oscillator with saw tooth type AFC, a Horizontal pre-driver with a X' ray protection circuit, a Vertical oscillator and a Vertical pre-driver in a 42-leads dual-in-line plastic package.

The TA7698AP realizes a very simple PAL CTV or a PAL/NTSC dual system CTV in conjunction with the TA7680AP/81AP PIF/SIF combination IC. And also to realize a PAL/SECAM/NTSC multi standard system CTV, a SECAM demodulator and a system switch are required in addition to the above two chips.

Followings are the operation discriptions based on the block diagram.

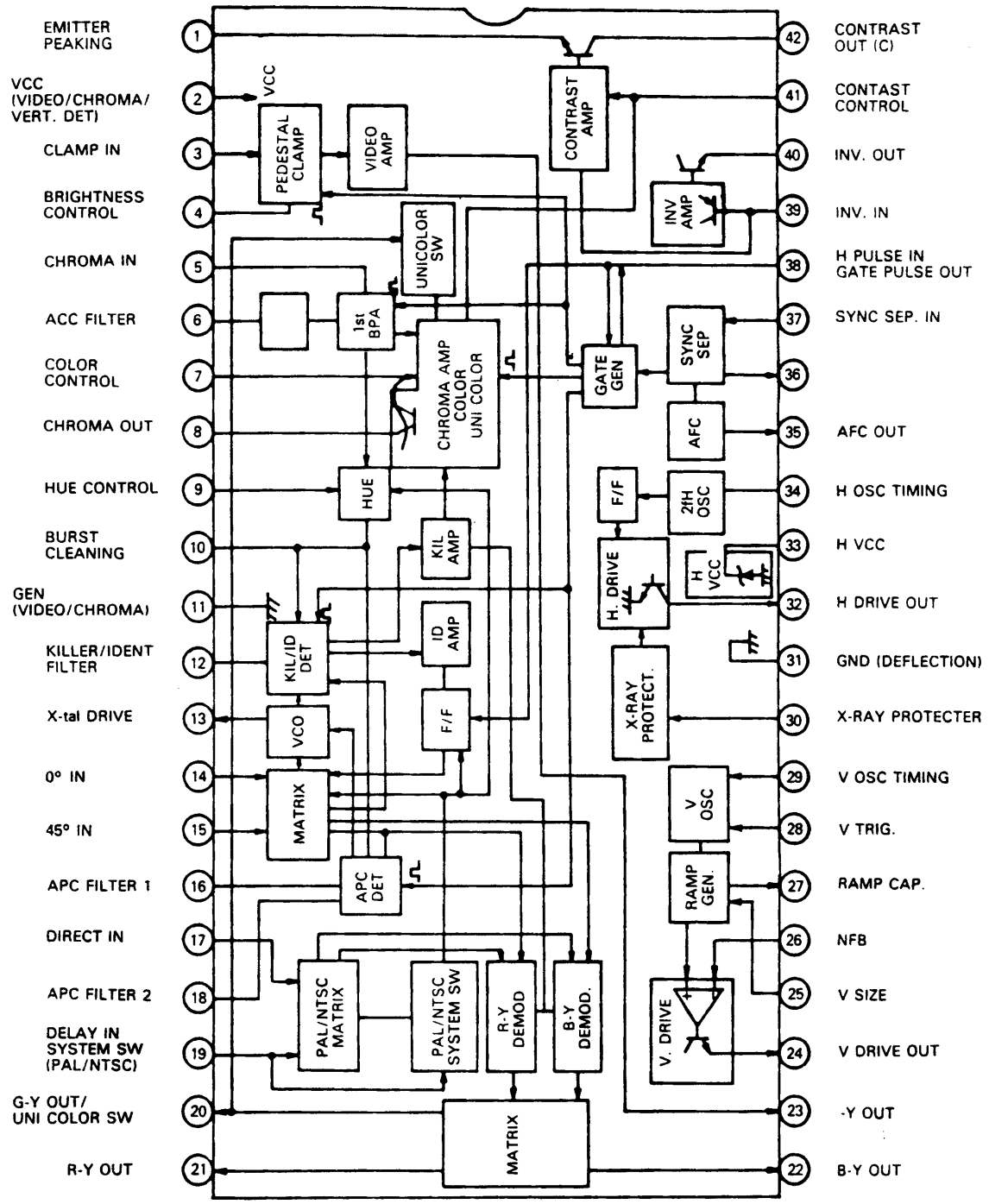
(2) Separation of the Vcc Lines and the GND Lines

The TA7698AP equipts with Vcc lines. One of them are the #2 terminal 12V line for the video chroma subsystem the sync separator and the vertical deflection system. The other is #33 8V Vcc line providing an internal zener regulator for the AFC and the horizon tal section. This 8V line is driven by the high +B line (+110V to +130V) through a series resistor to start up the system. After setting up the system operation, current from the 12V Vcc line maintains this 8V line power requirement.

And also the TA7698AP equipts separated GND lines. To prevent inter-section interferences each section has it's one GND line. The lins are tied together at the IC GND pad to reduce common impedances. The #11 terminal is a GND line for the video section and the chroma demodualtor, and the #31 terminal is another GND line for the sync separator and the deflection system.

These GND lines are pulled out to each side of the IC package to be minimize the common impedance. Special attentions should be payed to a pattern layout of the external GND line.

TA7698AP BLOCK DIAGRAM



(3) Video Section

(a) Inverter Amplifier

The composite video signal from the output of the PIF stage is applied to the inverter amplifier through a sound carrier trap

The #39 is the input terminal, and the operating bias is derived from the DC component of the PIF output. The input dynamic range is 2.0V to 6.5V typ., and a sync-negative comosite video signal input is required.

The #39 is also the input terminal of the contrast amplifier.

The output terminal of the inverter amplifier is the #40, and the output circuit is emitter follower construction to increase the driving capability. The inverted video output signal is applied to the sync separator and the chroma bandpass amplifier through a chroma signal taking out circuit. The typical gain of the inverter amplifier is 3.5dB.

(b) Contrast Amplifer

The input terminal of the contrast amplifier is also the #39, and a collecter output is the #42 and an emitter output is the #1. A frequency dependent circuit is connected to the #1 to obtain the picture control (Peaking Control) function.

The #42 collector output is applied to the pedestal amplifier through a video delay line with subcarrier trap to compensate the group delay difference between the chroma signal and the video signal. The required delay time will be 0.4uS to 0.7uS, and should be adjusted to be optimize the compensation.

The #41 is the control terminal of the contrast control. the minimum 40dB contrast control range is obtained by the #41 DC voltage change 2V to 10V.

When a 2.7kohm resister is connected between the #20 (G-Y Out) and GND, the contrast control also controls the color saturation (Uni-Color Control). And when the #20 is opened, the contrast control is independent.

In other words, when the three color differential outputs are used (PAL or PAL/NTSC application), the contrast control operate as the "Uni-color control". And when two of them, R-Y and B-Y, are used (PAL/SECAM/NTSC APPLICATION), only the contrast is controled. In the later case, a PAL-SECAM system switch IC will control the uni-color function.

(c) Pedestal Clamp Amplifier and the Video Output Amplifier

The output video signal from the contrast amplifier is applied to the pedestal amplifier. The brightness control and the DC restoration (Pedestal Clamp) functions are in this stage.

The processed video signal is fed to the #23 (-Y output).

The #4 is the brightness control terminal. The ABL (Automatic Brightness Limitting) functions is realized also by this terminal.

The DC restoration ratio is variable by superposing the video signal of the #3 to the #4 brightness control terminal.

An PNP transistor is connected between the #23 (-Y output) and the chroma output stage to minimize a switch-on drifting that may be caused by the thermal capacity difference between the IC and the chroma output transistors.

The maximum output amplitude of the #23 (-Y output) is 7.5Vp-p typ. (10% to 90%), and the DC restoration ratio is 70% typ. by external components values given in the block diagram.

(4) Chroma Section

As the TA7698AP provides a CCIR axis PAL chroma demodulator and a NTSC axis NTSC chroma demodulator controled by an internal PAL/NTSC system switch, it realizes wide capability of applications.

(a) The 1st Chroma Bandpass Amplifier

The inverter amplifier output from the #40 is applied to a chroma bandpass filter to take out the chroma information. The chroma signal is applied to the #5 the 1st chroma bandpass amplifier input. The #5 terminal is biased internally.

The 1st chroma amplifier detects amplitude of the burst signal gated from the chroma signal by the burst gate pulse, and controls it's gain to obtain constant burst signal level chroma output (ACC: Automatic Chrominance Control).

The recommendable input level of the #5 (Burst level) is 120mVp-p.

A typical ACC characteristics is shown below.

The #6 is the ACC time constand terminal to detect the burst level.

(b) Chroma Amplifier

The #8 is an emitter follower output terminal of a chroma signal, of which burst component is drawn out by the burst gate and the saturation level is controled by the color control and the uni-color control.

The #7 is a control terminal of the color saturation (chroma amplitude). The control characteristics is shown bellow.

The chroma output of the #8 is applied to the #17 direct signal input, and to the #19 delayed signal input. The amplitude and the phase relation of these two chroma signal sould be adjusted by the external circuits.

(c) Tint (Hue) Control

In case of the NTSC mode, the #9 is a control terminal of the color tint (or hue) by shifting the burst phase applied to the APC circuit. In the PAL mode, this terminal sould be grounded by a capacitor to prevent interferences.

(d) Killer/Ident Detector, Flip-flop

Detecting the burst signal level, the killer detector switches off the operation of the APC and the chroma demodulator (forced B/W mode) when the level is lower than the designed value. And also the ident detector normalizes the phase of the flip-flop driven by the horizontal flyback pulse when in PAL mode.

The #12 is the terminal of a time constant of the killer and ident dtector, and the DC level $V_{\#12}$ to the detectors.

When the B/W signal reception, the $V_{\#12}$ is 8V typ.. And when the color signal is received $V_{\#12}$ increases and killer operation is released.

When there is a disagreement between the PAL burst phase alternation and the flip-flop phase the $V_{\#12}$ decreases and the ident detector normalizes the flip-flop to correct the chroma demodulation.

The #10 the burst cleaner (a tank circuit tuned to the sub-carrier frequency) is connected to the inputs of the detectors to feed a clean brust signal to the detectors. And it is possible to introduce a constant phase shift between the chroma signal and the burst signal by the tank alignment.

(e) APC Detector, VCO, Matrix Circuit

The APC detector and the VCO (or VCXO Voltage Controled X'tal oscillator) generate a sub-carrier frequency coinsident to the burst phase. The phase difference between the output of the VCO and the burst is detected by the APC (Automatic Phase Control) detector and the output controls the frequency and the phase of the VCO. The #16 and the #18 are the APC filter terminals.

The free running frequency of the VCO is adjusted by a trimmer capacitor connected a X'tal in series or a potentio-meter in the APC filter.

The matrix composes the R-Y/B-Y demodulator reference signals having the required phase difference between the burst signal.

(f) PAL/NTSC Matrix, PAL/NTSC System Switch

In PAL mode, the direct signal is applied to the #17 and the delayed signal to the #19. These signals should have the same amplitude and dthe correct phase relation.

The PAL matrix composes the continuous R-Y and B-Y color signals by adding or subtracting the two signals from the #17 and the #19, and reduces the cross-talk between the signals.

The R-Y and the B-Y signals are fed to the chroma demodulator.

In NTSC mode, the input is only the #17, and the NTSC matrix adjust the R-Y and the B-Y color level to the PAL mode's to keep the same demodulated color outputs.

Above mode change is controled by the DC voltage of the #19.

When the V#19 is lower than 2V, the PAL/NTSC system switch turns the system to the NTSC mode. (Actually, only the #19 may be grounded to change the switch.)

The differences between these two modes are listed bellow.

	Relative Amplitude		Relative Phase	TINT	F/F
	B-Y/R-Y	G-Y/B-Y			
PAL	1.78	0.58	±90°	OFF	ON
NTSC	0.95	0.31	105°, 235°	ON	Stop

(g) R-Y, B-Y Demodulator, G-Y Matrix

The R-Y, B-Y color signals from the PAL/NTSC matrix are fed to the R-Y and B-Y chroma demodulator, and demodulated.

The G-Y matrix composes the G-Y color differential signal from the demodulated R-Y and B-Y color differential signals.

These three color differential signals are fed to the chorma output circuit through the CR carrier filters from the #20, #21 and #22 output terminals.

In the chroma output circuit, these color differential signals are matrixed with the -Y luminance signal from the #23 to obtain the R, G and B color primally signal driving a C-CRT.

For the SECAM mode of the multi-system, the #20 G-Y terminal is opened to stop the uni-color function.

(5) Deflection Section

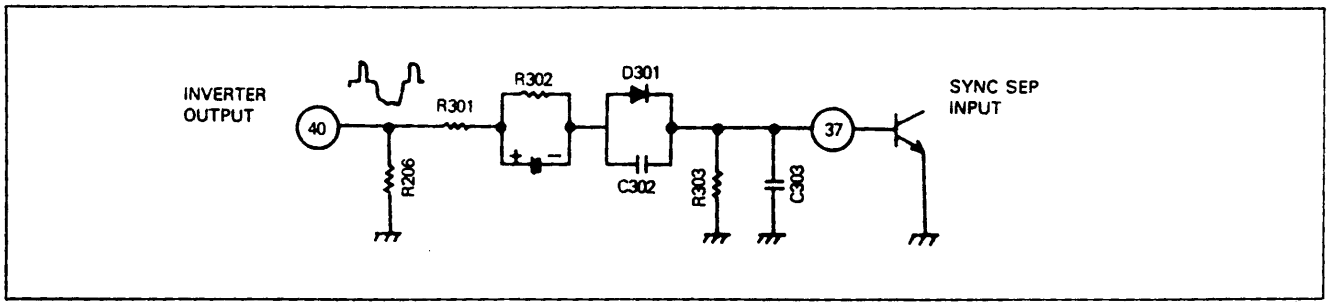
The deflection section of the TA7698AP includes a sync separator, a saw tooth type horizontal AFC, a horizontal oscillator, a horizontal pre-driver with an X'ray protecter, a vertical oscillator and a vertical pre-driver.

The GND line of this section is separated to the other, but the Vcc line except the AFC and the horizontal section is common to the other sections.

(a) Sync Separator

The #37 is an input terminal of the base-time constant type sync separator. The composite video signal from the #10 (Inverter output) is applied through a sync separator time constant circuit.

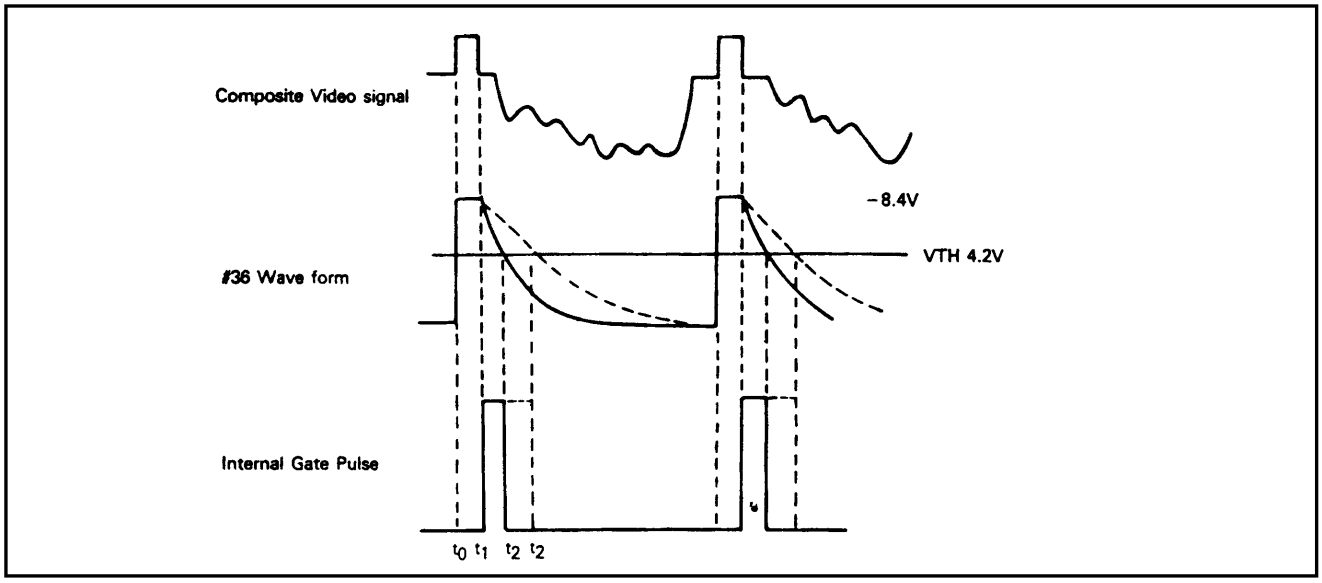
The slice levels of the horizontal sync and the vertical sync can be set independently.



R206 ..... #40 load resistor
R301, R303, C302 ..... Determines horizontal sync slice level
R301, R302, R301 ..... Determines vertical sync slice level
D301 ..... Time constant separation
C303 ..... Noise filter/Gate pulse rising edge timing

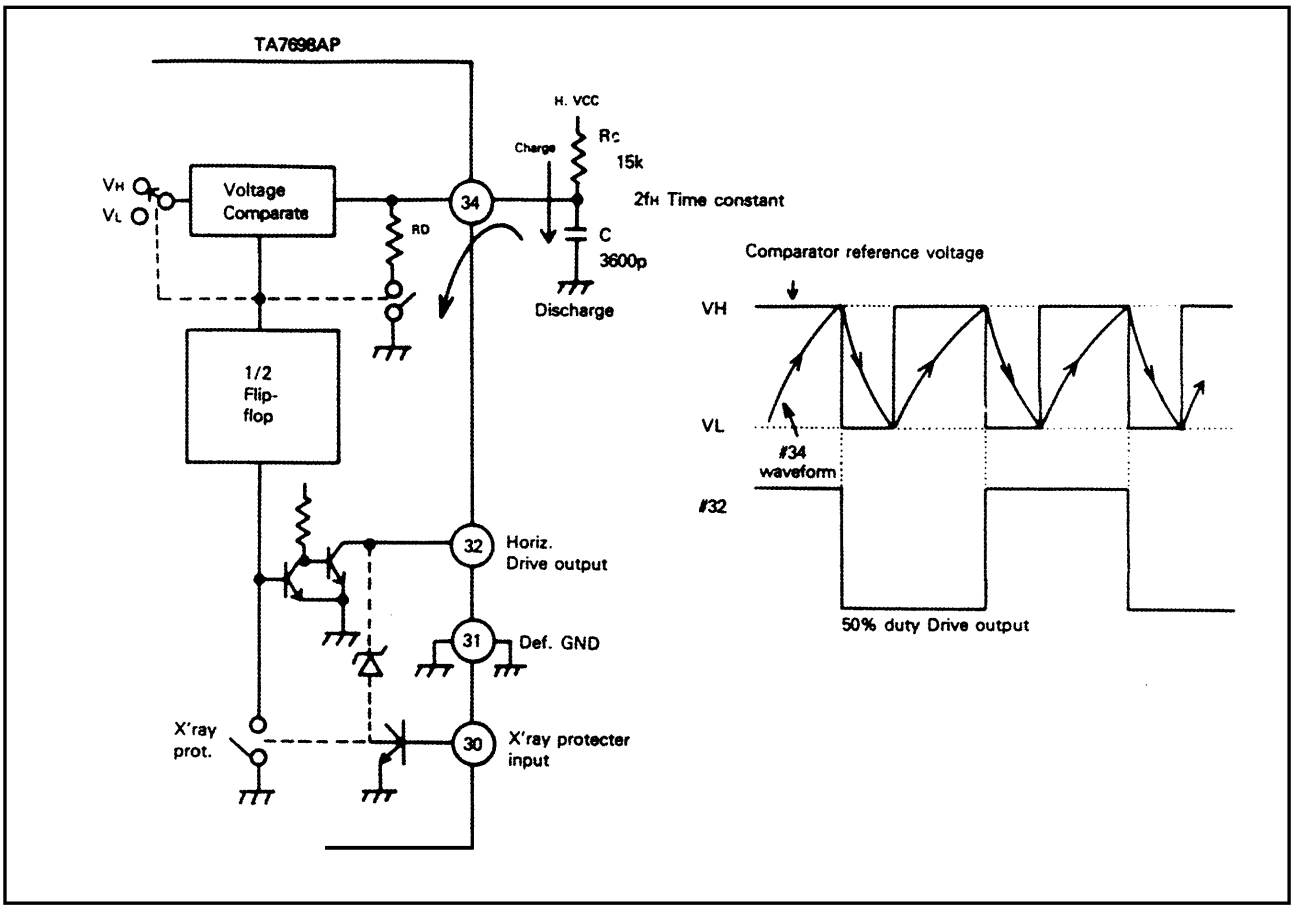
To deepen the slice level;
Horizontal : R301 incrase or R303 decrase
Vertical : R301 increase or R302 decrase

The #36 is the output terminal of the sync separator, and also this terminal is used as a time constant of the internal gate pulse generation.



The rising edge of the gate pluse t_{1l} is determined internally but little adjustment is possible by the change of C303 connected between the #37 sync separator input and the GND.

The folling edge of the gate pulse t_{2l} is determined by an external integration time constant connected to the #36 terminal



Special attention sould be payed to the pattern layouting and wiring of the #32 horiz. drive circuit and the #31 Deflection GND line because these are large f_H component current pathes.

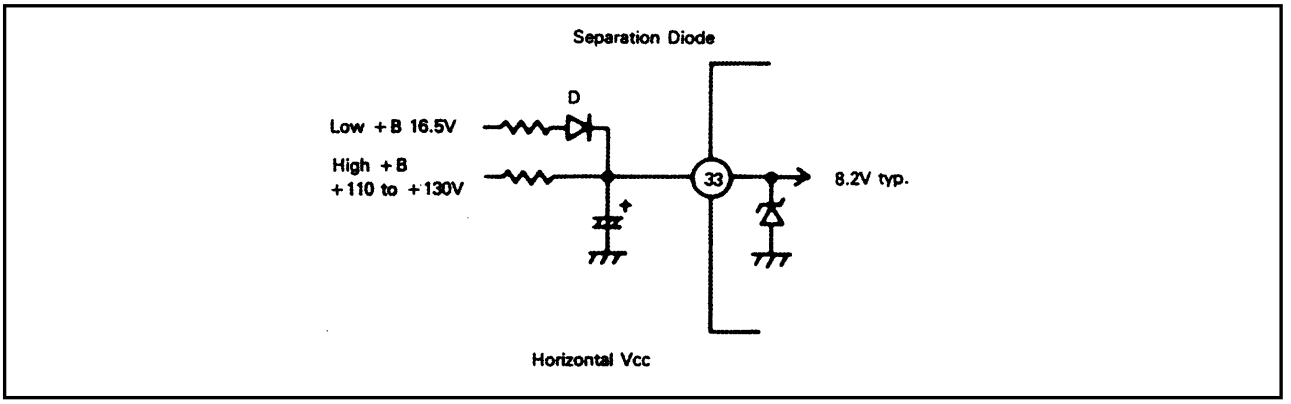
The horizontal drive circuit provides an SCR type X'ray protecter to prevent X'ray radiation from the CRT. The X'ray protecter will operate when the EHV (Extreamly High Voltage for CRT operation) exceeds certain value, and that is determined by external components. Also the X'ray protecter will operate when the #32 voltage exceeds 8.6V typ..

When the X'ray protecter operates the #32 output is shut down to the GND level, and it will not recover before re-switching the power supply.

(d) Horizontal Vcc

As described previously, the supply voltage of the horizontal section is applied from a zener type voltage regulator as shown bellow. When a CTV set is switched on, some supply current which is required to starting up the horizontal section is supplied from the high +B line (+110 to +130V), and then an internal flyback pluse power supply (low +B line 16.5V or 12V) is activated and supports the supply current of the horizontal section.

The internal zener voltage is 8.2V typ.. A diode inserted low +B line is for separation between these two power supplies.



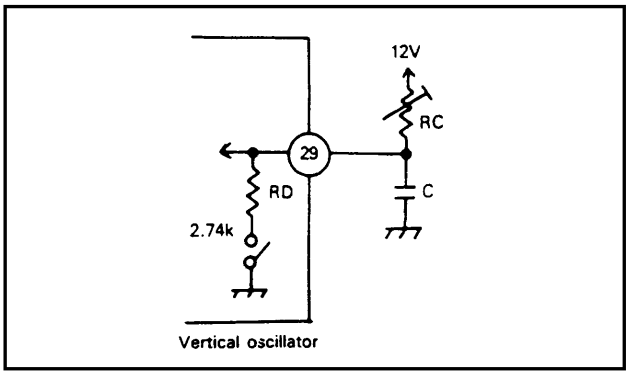
(e) Vertical Sync. Vertical Oscillator

The composite sync output from the #36 is integrated by the external time constant to obtain the vertical sync signal, and the sync signal is applied to the #28 vertical sync terminal.

The vertical oscillator is also an CR charge-discharge type as same as the horizontal oscillator.

The vertical sync pulse re-trigers the oscillation and pull in the frequency to vertical frequency fv.

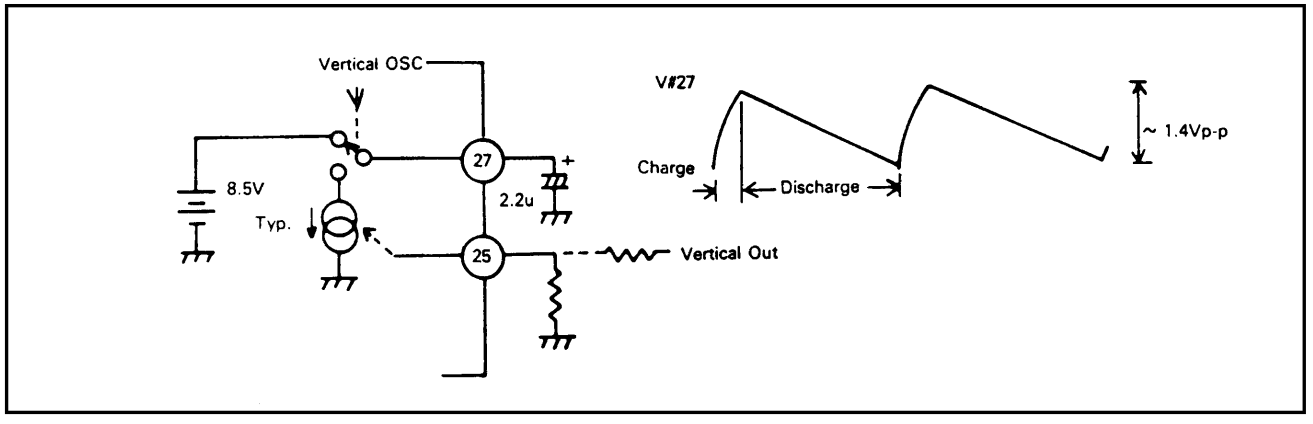
The #29 is for the oscillator time constant. The discharging resister RD is included in the IC. The vertical retrace time is determined by the time constant $C \cdot (RC/RD) = C \cdot RD$.



(f) Ramp Generator

A linear ramp wave is generated by constant voltage charging and constant current discharging a capacitor connected to the #27 terminal. The charge-discharge timing is controled by the vertical oscillator output. The diacharging current is determined by a resister connected to the #25 terminal.

As the vertical output amplitude is proportional to the #27 voltage amplitude, it is possible to compensate the vertical linearity by feeding back the output to the #25 terminal.



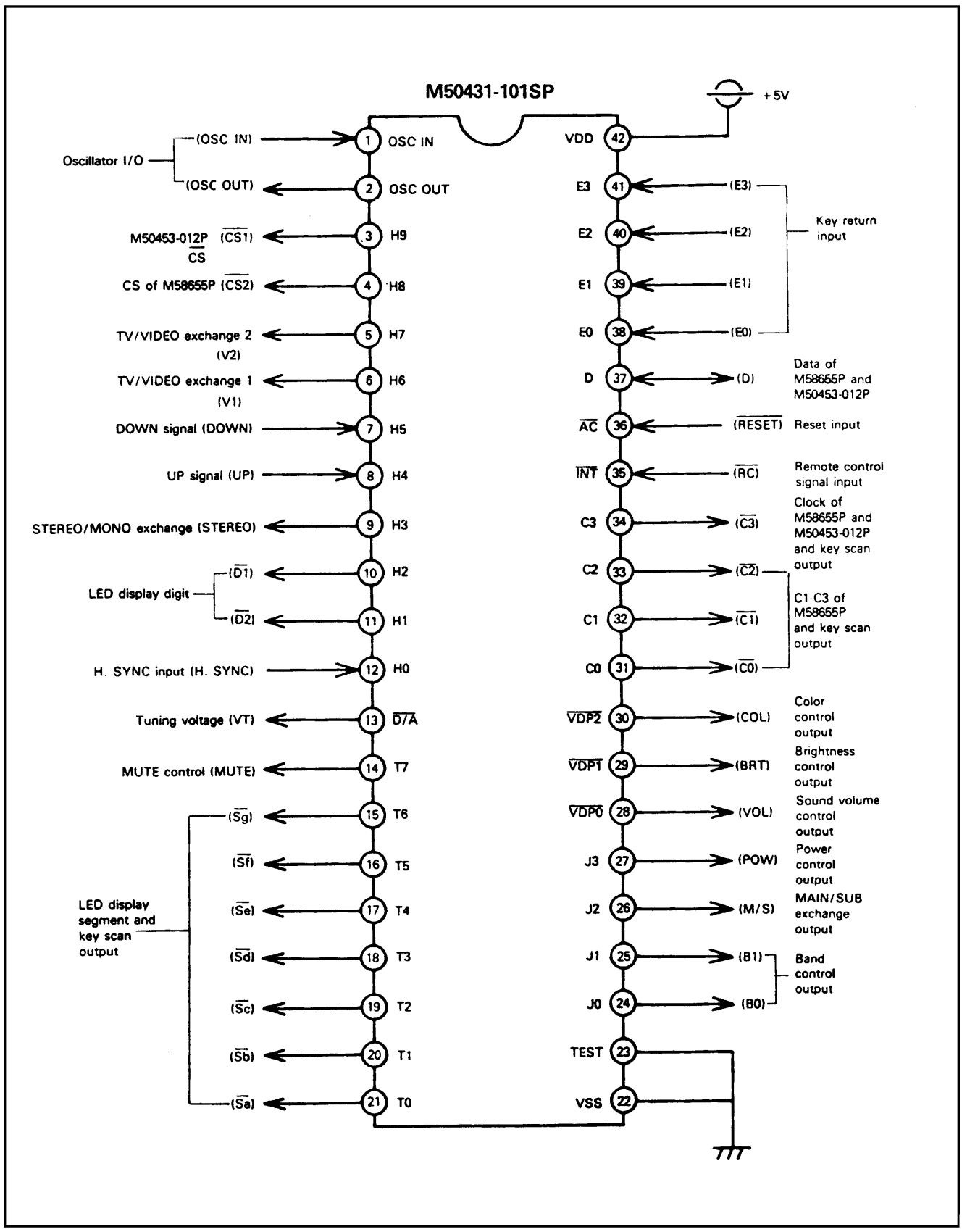
(g) Vertical Driver Amplifier and the Vertical Output Circuit

The vertical output section which is consist of the vertical drive NFB amplifier of the TA7698AP and an SEPP ar an SRPP output stage drives a vertical deflection coil DY so that the current wave form of the deflection coil DY will be similar to the ramp wave from at the #27. A series resister RS converts the DY current wave from to a similar voltage wave form.

And the voltage wave form and the output DC component are applied to the #26 NFB terminal through a ß circuit. The ß circuit determines the output current amplitude and the center voltage.

3. M50431-XXX SP

(1) Terminal Connection Diagram



(2) Terminal Description

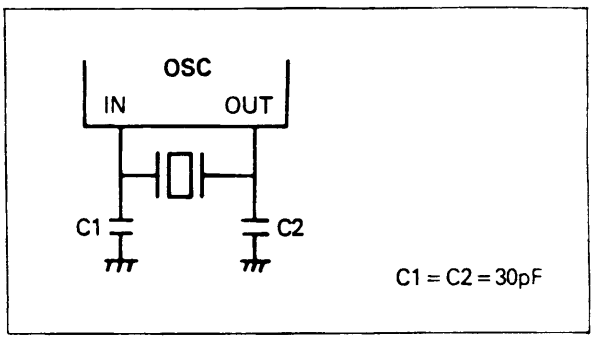
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Name</th><th>Function Explanation</th></tr>
<tr><td>1, 2</td><td>OSC IN
OSC OUT</td><td>Oscillator
Input/Output</td><td>By connecting the 4 MHz ceramic oscillator and capacitors between the terminals as shown below, the reference clock can be obtained. Since the constant of capacitors and so forth depends on the oscillator in use, use the recommended values of the manufacturer.


Fig. 5-1 Example of oscillating circuit by using a ceramic oscillator</td></tr>
<tr><td>3</td><td>SC1</td><td>Chip Select Output of M50453-012P</td><td>This is a chip select signal output terminal for on-screen display IC M5043-012P. The signal goes low when data is transferred to the M50453-012P.</td></tr>
<tr><td>4</td><td>CS2</td><td>Chip Select Output of M58655P</td><td>This is a chip select signal output terminal for an EAROM M58655P. This signal goes low when data is transferred to the M58655P.</td></tr>
<tr><td>5, 6</td><td>V2, V1</td><td>TV/VIDEO Exchange 1, 2</td><td>V1 and V2 are output terminals for exchangeing TV/VIDEO. TV/VIDEO exchanging is controlled by input of TV/VIDEO key as shown below.
<table><tr><th>Mode</th><th>V1</th><th>V2</th></tr><tr><td>TV</td><td>L</td><td>L</td></tr><tr><td>VIDEO 1</td><td>H</td><td>L</td></tr><tr><td>VIDEO 2</td><td>L</td><td>H</td></tr></table>When power is OFF, TV mode is set, and when the power is ON, start, start from TV mode.</td></tr>
<tr><td>7</td><td>DOWN</td><td>DOWN Signal Input</td><td>This is input of DOWN signal generated by comparing AFC siganl with the reference voltage, and use for auto-search and digital AFT operation. Input is in active "H".</td></tr>
<tr><td>8</td><td>UP</td><td>UP Signal Input</td><td>This is input of UP signal generated by comparing AFC signal with the reference signal, and used for auto-search and digital AFT operation. Input is in active "L".</td></tr>
<tr><td>9</td><td>STEREO</td><td>Stereo/Monaural Exchange Control Output</td><td>This is a sound exchange signal output terminal. This signal goes high after releasing reset. The signal state rolls over between high and low whenever the STEREO/MONO key is depressed.
High level ..... Stereo
Low level..... Monaural</td></tr>
<tr><td>10, 11</td><td>D1 and D2</td><td>Digit Output</td><td>These are digit signal output terminals for LED display. For the two digits display, outputs are as follows:
<table><tr><th></th><th>D1</th><th>D2</th></tr><tr><td>Upper digit ON</td><td>Low</td><td>High</td></tr><tr><td>Lower digit ON</td><td>High</td><td>Low</td></tr></table></td></tr>
</table>

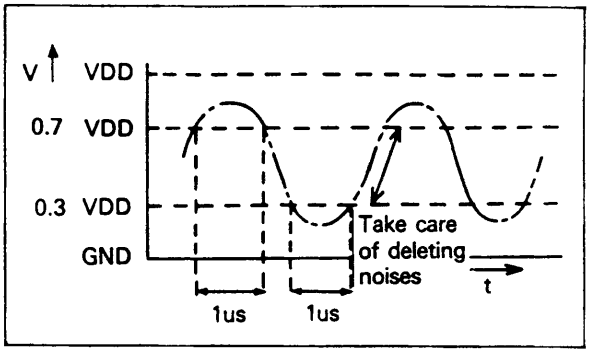
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Name</th><th>Function Explanation</th></tr>
<tr><td>12</td><td>H. SYNC</td><td>Horizontal Synchronous Signal Input</td><td>This is an input terminal for horizontal synchronous signal. Pulses entered into H. SYNC terminal are counted for approx.
1.02 ms and when the value of the counter is in the range from 14 to 24, existence of synchronizing signal is determined. The input conditions are as follows:


Fig. 5-2 Input conditions of horizontal synchronous signals.

Keep the settled levels of low and high states for more than 1 us.
In addition, take care of noises around input threshold voltage.</td></tr>
<tr><td>13</td><td>VT</td><td>Tuning Voltage Control</td><td>This outputs a waveform which is modulated bys the pluse-width in accordance with 14-bit digital information.</td></tr>
<tr><td>14</td><td>MUTE</td><td>Mute Control Output</td><td>This is a sound mute control output terminal. This signal is active high. This terminal is automatically controlled when the device is powered on/off, the program is selected, TV/VIDEO is exchanged, MAIN/SUB is exchanged, STEREO/MONO is exchanged, and during auto-search operation.
Besides, if the cycle disappears during slow digital AFT, "H" is set automatically. (MUTE ON state is set.)
* When the MUTE key is depressed, this port is not changed.</td></tr>
<tr><td>24, 25</td><td>B0 and B1</td><td>Band Control Output</td><td>These are control band signal output terminals for a tuner. Assignment for bands is as follows:

Table 5-2
<table><tr><th>B0</th><th>B1</th><th>Band</th></tr><tr><td>L</td><td>L</td><td>VHF-L</td></tr><tr><td>H</td><td>L</td><td>VHF-H</td></tr><tr><td>H</td><td>H</td><td>CATV</td></tr><tr><td>L</td><td>H</td><td>UHF</td></tr></table></td></tr>
<tr><td>26</td><td>M/S</td><td>MAIN/SUB Exchange Output</td><td>This is an exchange signal output terminal of MAIN/SUB. This signal goes high when the device id powered on. This terminal is controlled by the MAIN/SUB key. Whenever the key is depressed, the signal rolls over between low and high.

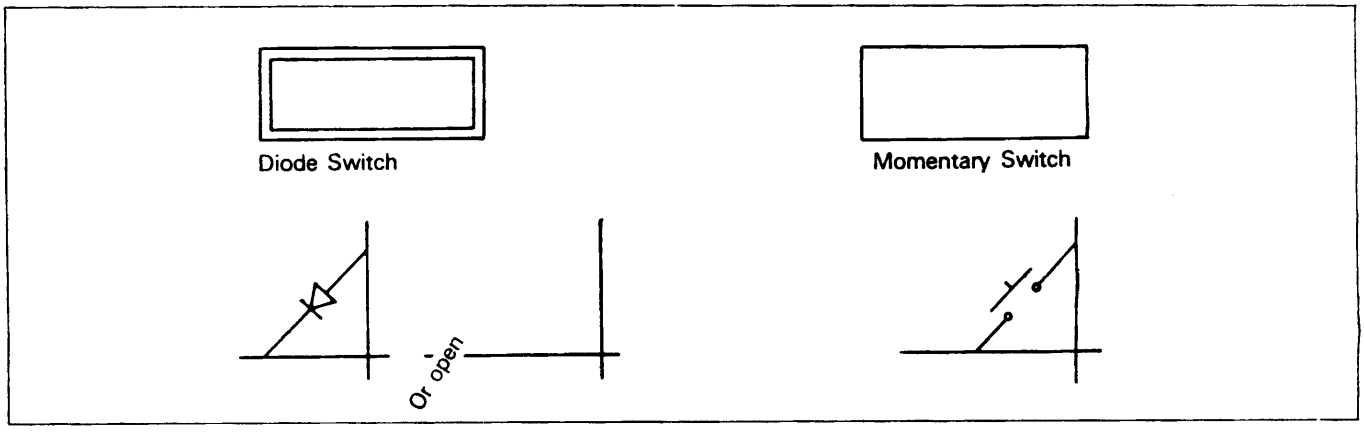
High level ..... Main
Low level..... Sub</td></tr>
</table>

Pin No.	Symbol	Name	Function Explanation
27	POW	Power Control Output	This is a power control terminal, which serves to control an external relay. This output is active high and when the reset function is operated, it reads POWER ON START key at approx. 20 ms after releasing reset. If POWER ON START key is ON, the power immediately turns ON, and if the key is OFF, the power is off until POWER ON/OFF key input. This output state rolls over between high and low whenever the POWER ON/OFF key is depressed. High level ..... Power ON Low level..... Power OFF In addition, if the off-timer is set, when the timer setting time elapses, the signal automatically goes low.
29, 30	BRT and COL	Brightness Control Output and Color Control	These are brightness and color control terminals. These output a waveform modulated bys the pulse width with 64 levels in accordance with 6-bit latch data (active low). When it is powered on, values before the device is powered off are read out from the EAROM and output to each port.
28	VOL	Sound Volume Control Output	This is sound volume control terminal (active low). The MUTE flag provided in the M50431-101SP allows the signal to immediately go high. For other specifications and output waveform, see the section of "BRT and COL".
30~33	C0~C2	C1~C3 Output of M58655P and key scan output	These are terminals for mode control of EAROM M58655P and key return signal source output terminals for key matrix.
34	C3	Clock Output for M58655P and M50453-012P and key scan output	This is a clock output terminal for an EAROM M58655P and on-screen display IC M50453-012P. Connect this terminal to the CLK of the M58655P and CK of the M50453-012P and key return signal source output terminals for key matrix.
35	RC	Remote Control Signal Input	This is a remote control signal input terminal. A remote control signal is acknowledged by sensing its edge. When a signal applied at the RC terminal goes high, the remote control signal reception operation is executed. The remote control signal input decision circuit includes a noise reduction circuit, which serves to delete less than 64 us pulses as noises. It can prevent malfunction of the device due to noises.
36	RESET	Reset Input	By adding the circuit as shown in Fig. 5-5 to the RESET terminal, when the device is powered on, the reset function can be activated. In addition, a Schmitt circuit is provided at the RESET terminal. although the reset is released at the time RESET terminal voltage Vc exceeds the threshold voltage VTH1, once released, unless Vc drops at the threshold voltage lower than VTH2, the reset function cannot be activated again. In addition, to securely activate the power-on reset function, it is necesary to set the time Vc is larger than VTH1 is more than 1 ms after the power supply voltage VDD becomes more than 4.5V Figure 5-6 shows.
37	D	Data Input/Output of M58655P and M50543-012P	This is an input/output terminal for EAROM M58655P or output terminal for on-screen display IC M50453-012P. Connects this terminal to the I/O of the M58655P and to the Ao of the M50453-012P.
38~41	E0~E3	Key Return Input	This is a key return signal input for the key matrix.
42	VDD	Power Supply Terminal	Connect this terminal to the 5V power supply.

(3) Structure of Key Matrix

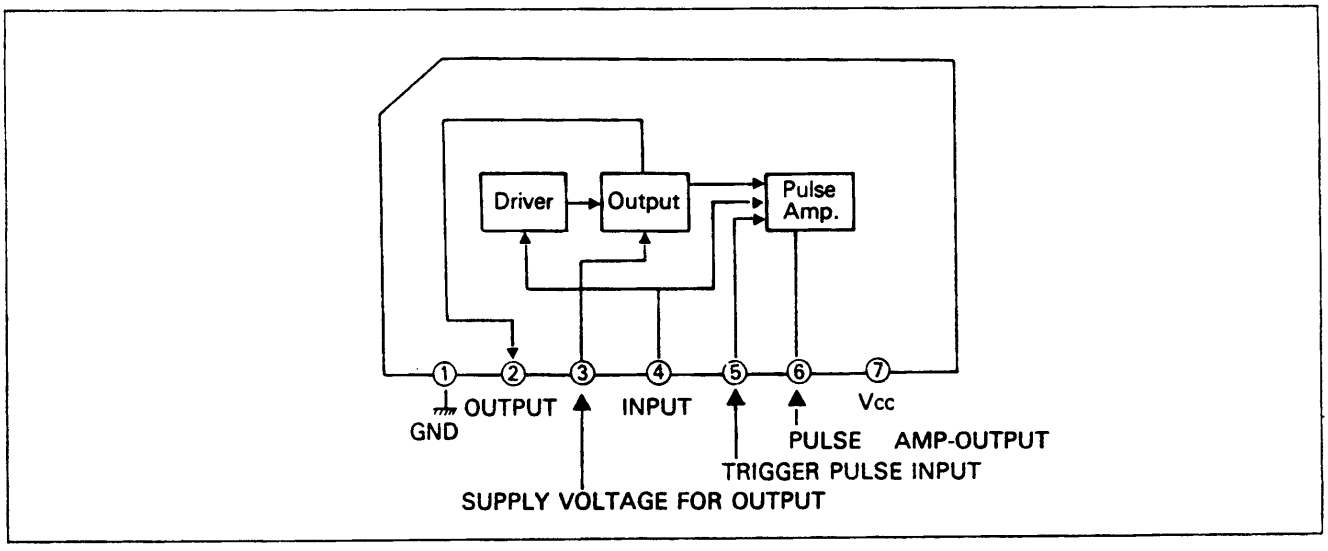
Input / Output	E0 (38)	E1 (39)	E2 (40)	E3 (41)
Sa (21)	PR (+)	VOL (+)	BRT (+)	COL (+)
Sb (20)	PR (−)	VOL (−)	BRT (−)	COL (−)
Sc (19)	POWER ON/OFF	TV/VIDEO	MAIN/SUB	STEREO/MONO
Sd (18)	FT (+)	FT (−)	MUTE	PR CALL
Se (17)	AS (+)	AS (−)	AFT ON	
Sf (16)	30 PR	12 PR	8 PR	
Sg (15)	1 BAND	4 BANDS	1 VIDEO/2 VIDEO	POWER ON START
C0 (31)	PR 1	PR 2	PR 3	PR 4
C1 (32)	PR 5	PR 6	PR 7	PR 8
C2 (33)	PR 9	PR 10/PR 0	PR 11/PR 1*	PR 12/PR 2*
C3 (34)	PR 13	PR 14	PR 15	PR 16

( ) Terminal numbers are represented in parentheses.



4. AN5515

(1) Block Diagram



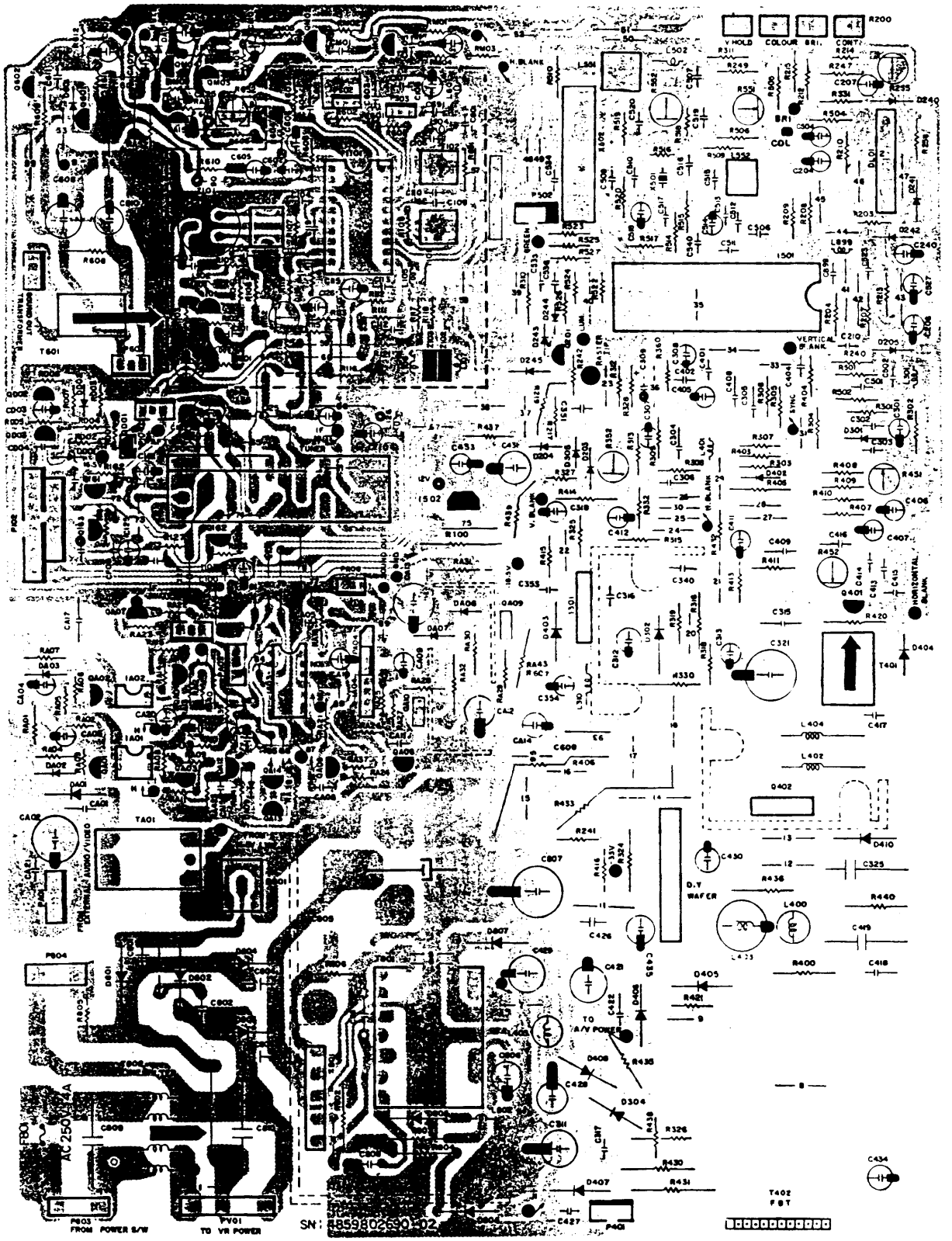
5. IC VOLTAGE CHART

NOTE: VOLTAGE MEASURED UNDER STANDARD COLOR BAR SINGAL INPUT.

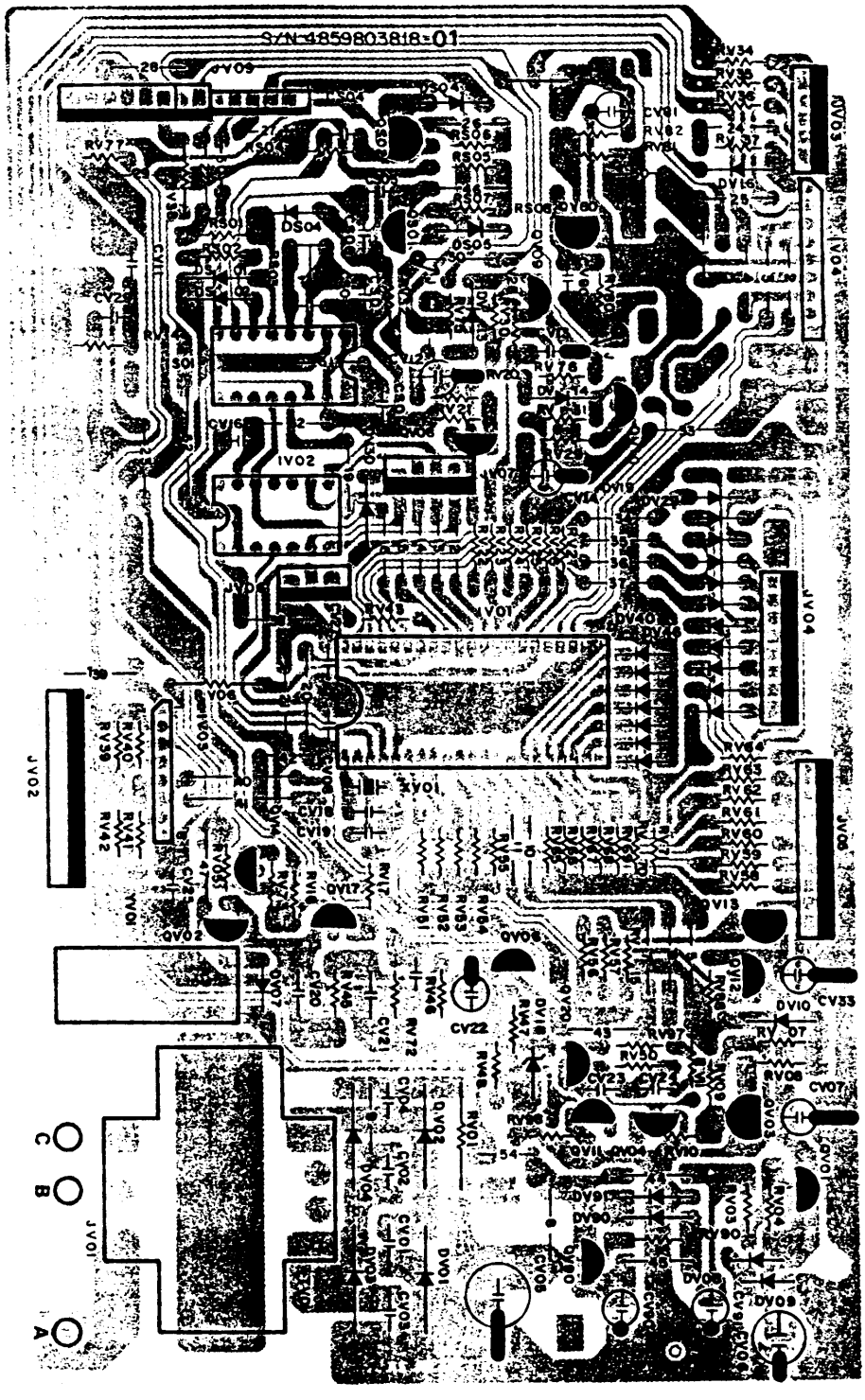
LOCATION	IC TYPE	VOLTAGE (PIN NO.)															
I 101	TA7680AP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		6.3	2.7	6.8	0	7.3	4.6	4.6	4.6	4.6	6.4	3.9	0	7.2	5.8	3.6	4.1
		17	18	19	20	21	22	23	24								
		7.7	4.1	7.7	11.5	4.1	4.4	5.3	4.5								
I 501	TA7698AP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		4.2	11.3	4.25	4.2	1	9.0	5.0	9.3	5.7	7.1	0	8.6	9.0	3.3	3.3	7.8
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
		3.8	8.0	3.9	7.6	6.9	6.9	6.3	0.5	3.74	7.9	7.9	0.44	2.6	—	0	0.4
		33	34	35	36	37	38	39	40	41	42						
		8.5	4.8	4.9	3.3	—	—	2.8	—	6.8	7.1						
I 001	M50431 —XXXSP	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		2.1	2.1	4.8	4.8	0	0	0	4.8	0	4.8	3.0	4.0	3.2	0	3.0	2.7
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
		1.5	—	—	—	—	0	0	—	—	—	4.6	4.9	11.5	11.5	—	—
		33	34	35	36	37	38	39	40	41	42						
		—	—	4.7	5.3	—	2.9	4.8	4.8	3.2	4.8						
I 301	AN 5515	1	2	3	4	5	6	7									
		0	—	25	6	0	3	25									

PRINTED CIRCUIT BOARDS

*COMPONENT VIEW OF MAIN BOARD

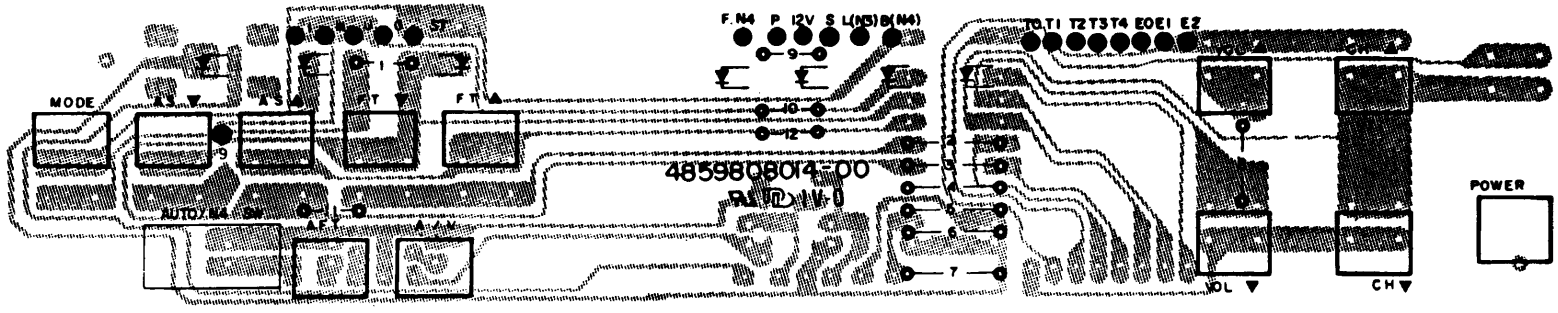


*COMPONENT VIEW OF RECEIVED BOARD

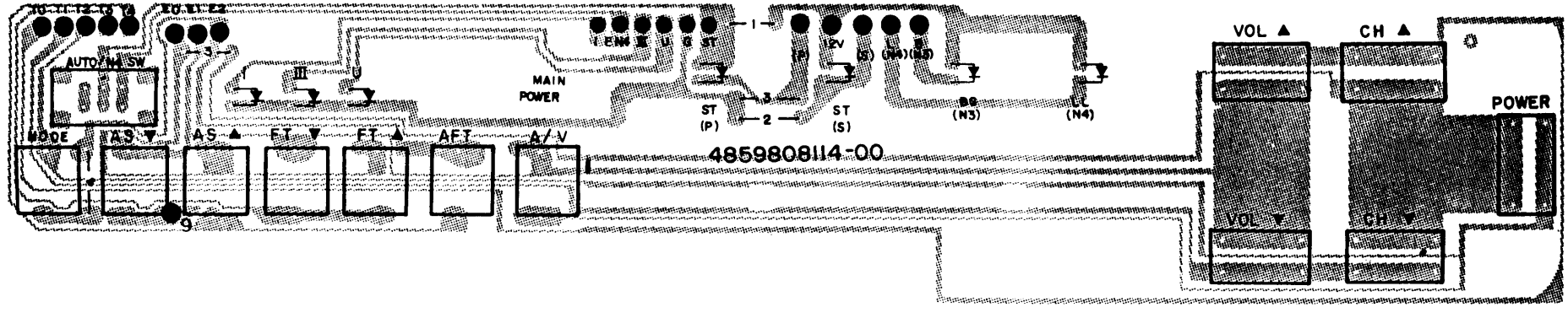


COMPONENT VIEW OF CONTROL BOARD

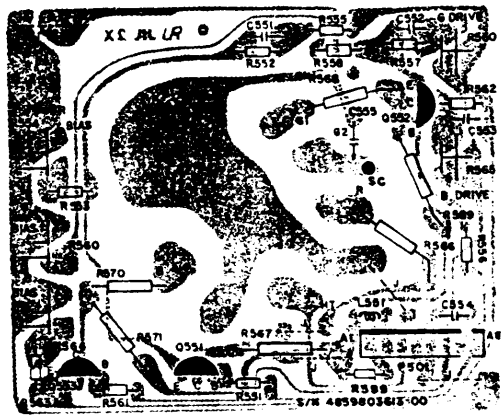
1) 14 INCH



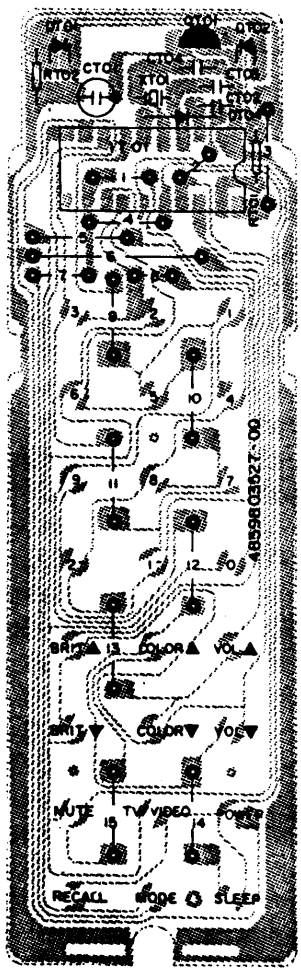
2) 20 INCH



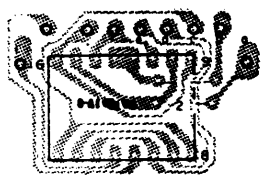
*COMPONENT VIEW OF CRT BOARD



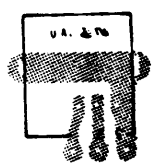
COMPONENT VIEW OF TRANSMITTER BOARD



COMPONENT VIEW OF CH DISPLAY BOARD

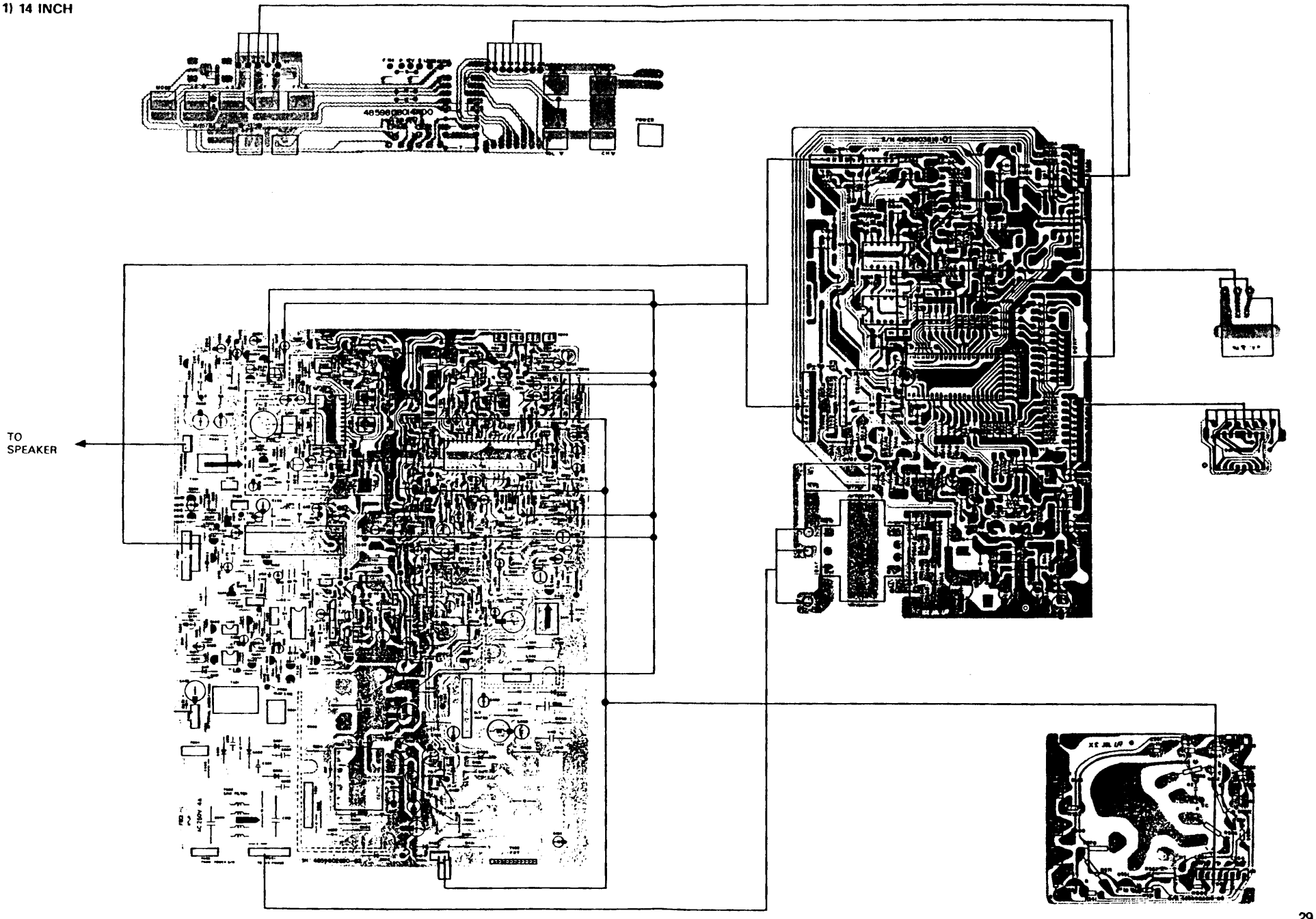


COMPONENT VIEW OF PRE-AMP BOARD



WIRING CONNECTION DIAGRAM

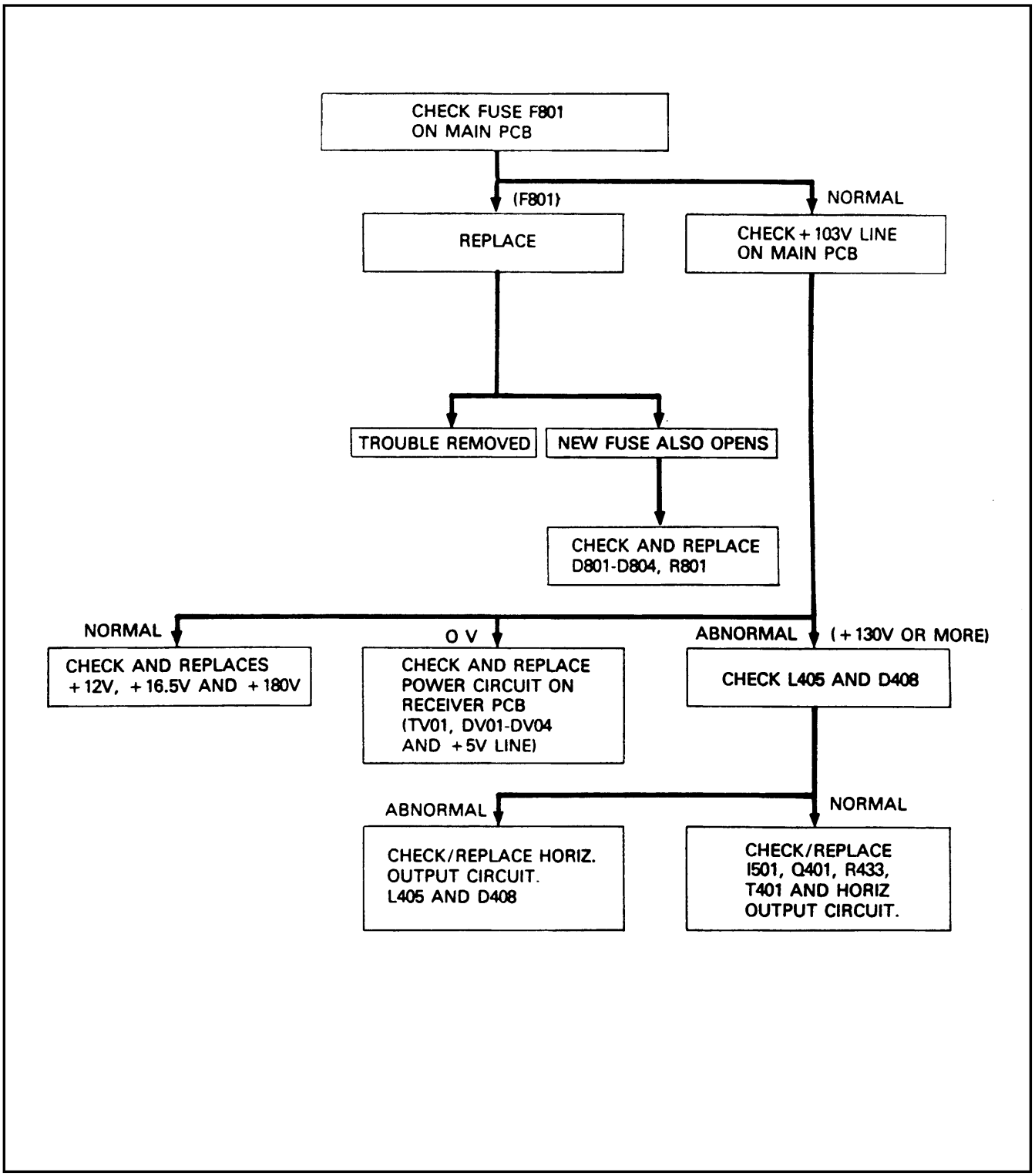
1) 14 INCH



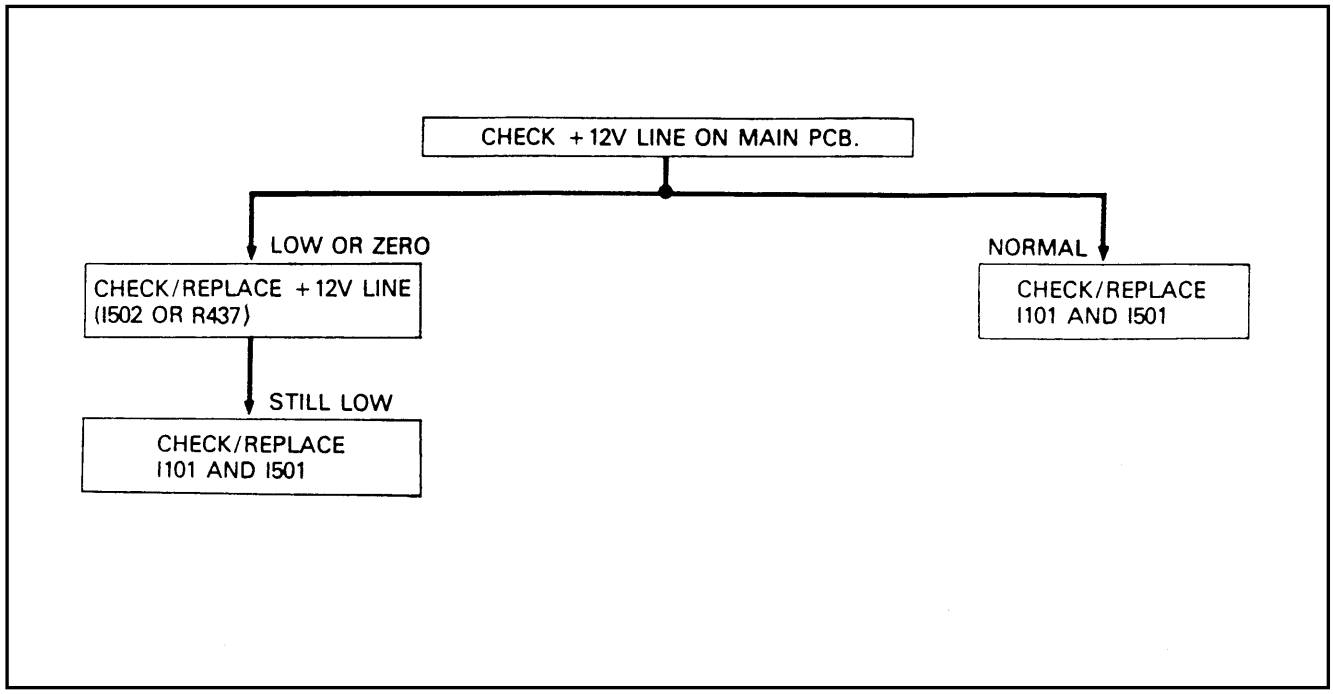
TROUBLESHOOTING CHARTS

The following charts are devoted to troubleshooting which, if followed carefully, will assist you in tracking down a fault to the correct stage.
In order to utilize the charts (fault trees), firstly establish the complaint, i.e.—No Raster, No Sound.
Locate the chart applicable and then progress through the various alternatives until a final block indicates the offening components or stage.

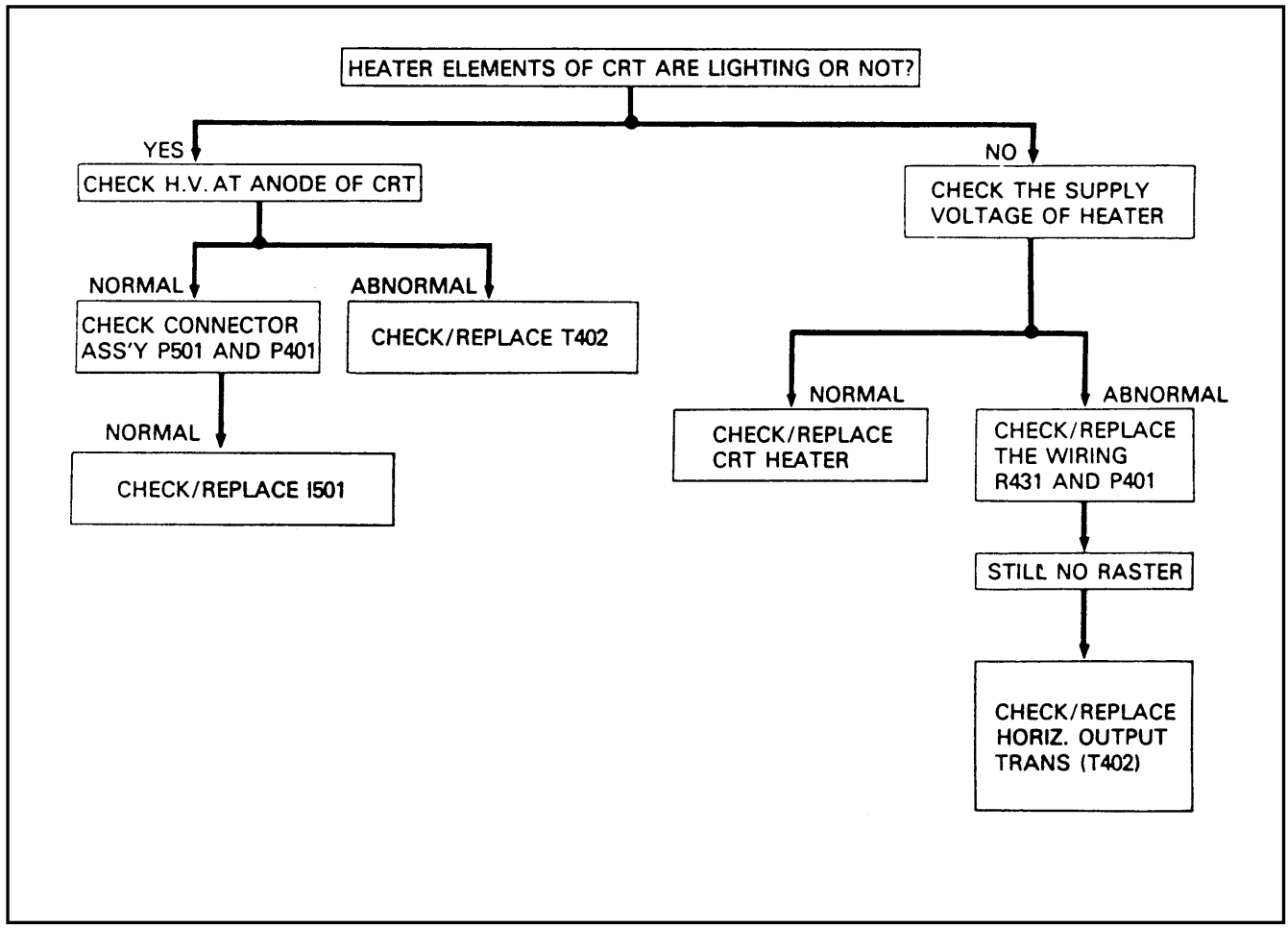
1. POWER FAILS TO TURN ON. (NO RASTER, NO SOUND, NO ATTEMPT TO TURN ON)



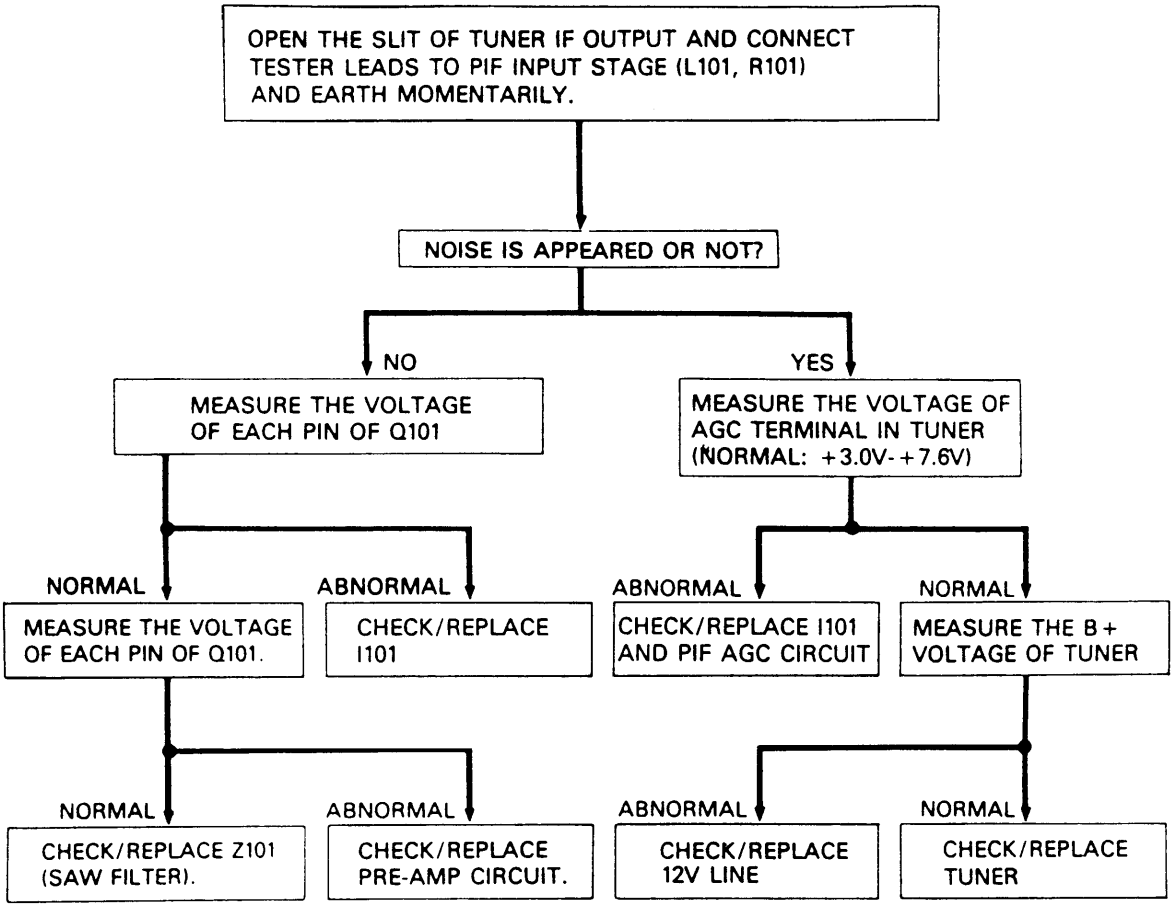
2. NO RASTER (SOUND NOISE OR WEAK)



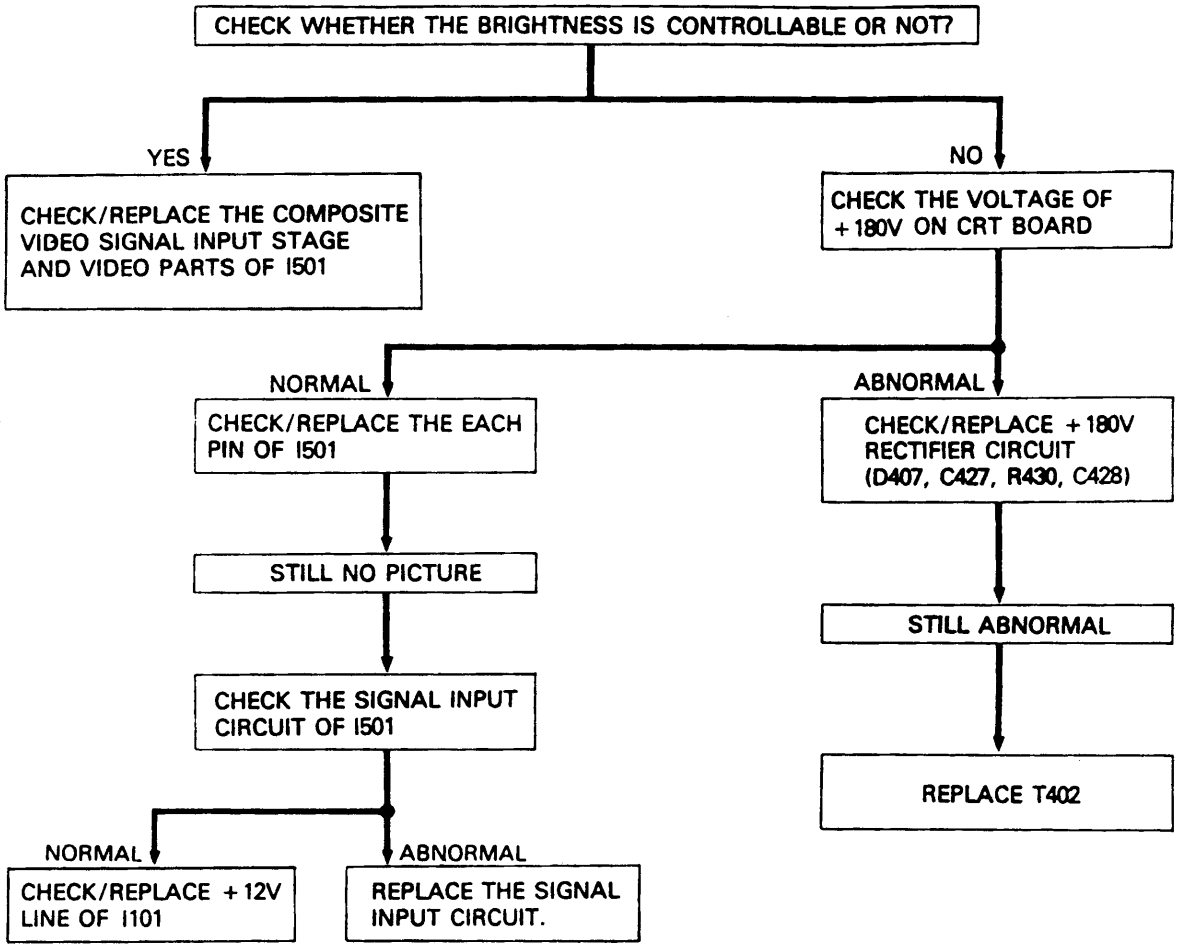
3. NO RASTER (SOUND OK)



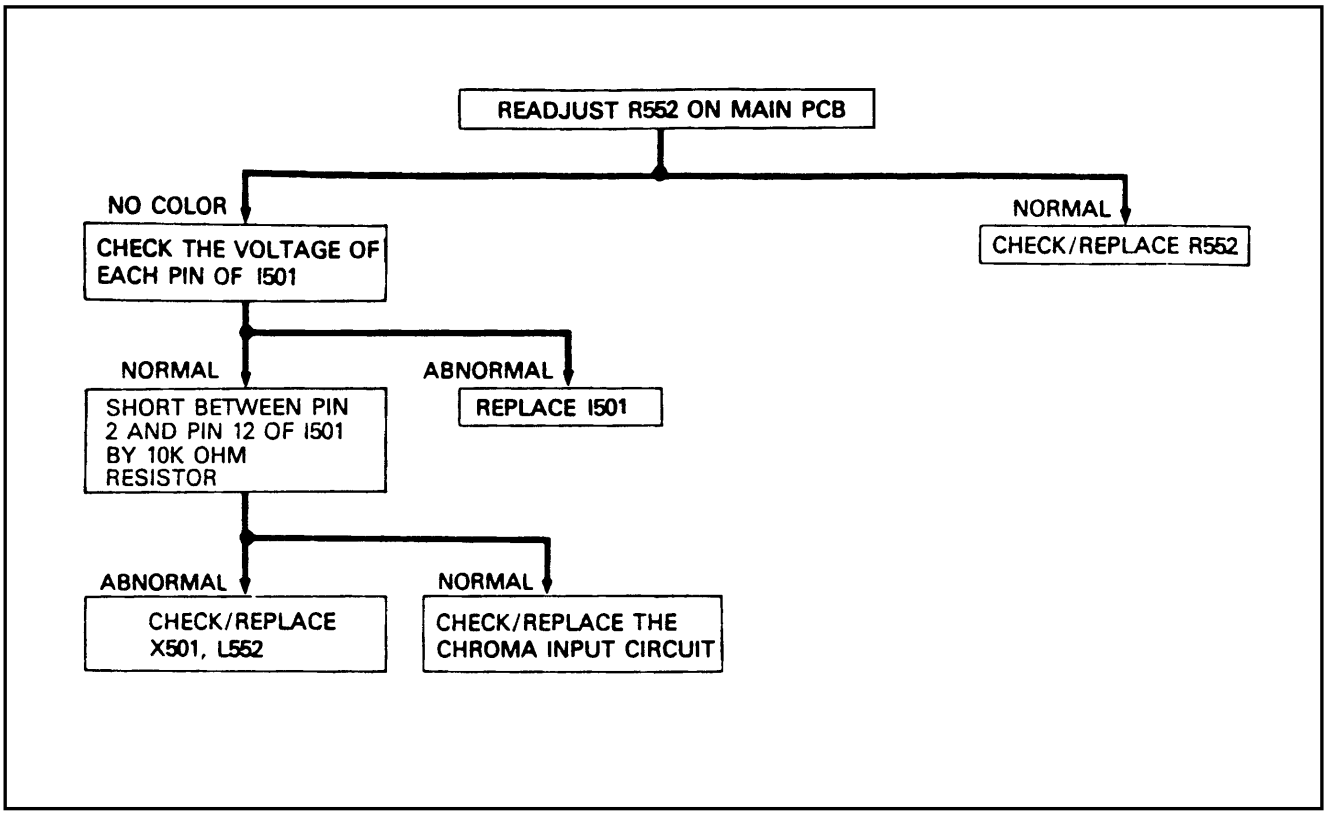
4. NO PITCTUR (RASTER REMAIN) AND NO SOUND)



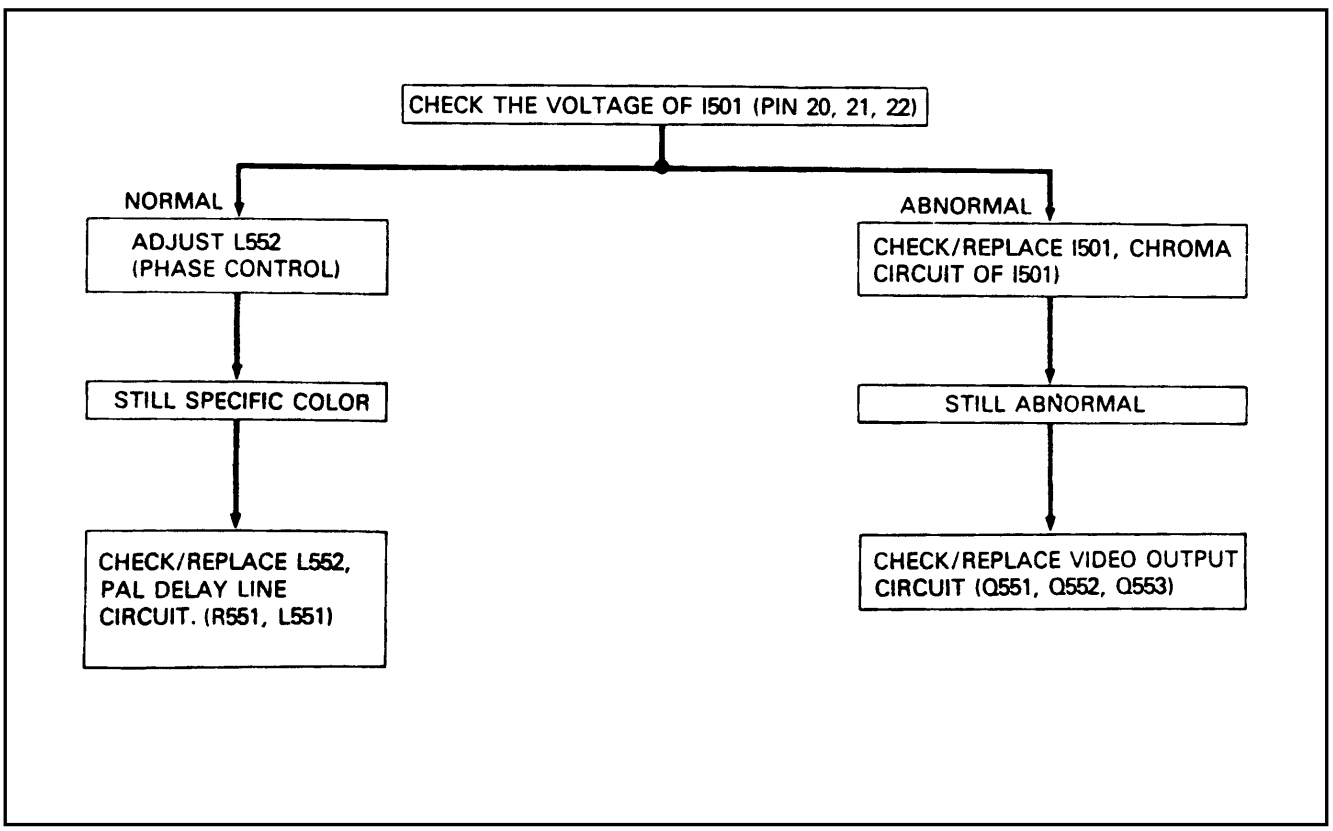
5. NO PICTURE (RASTER AND SOUND OK)



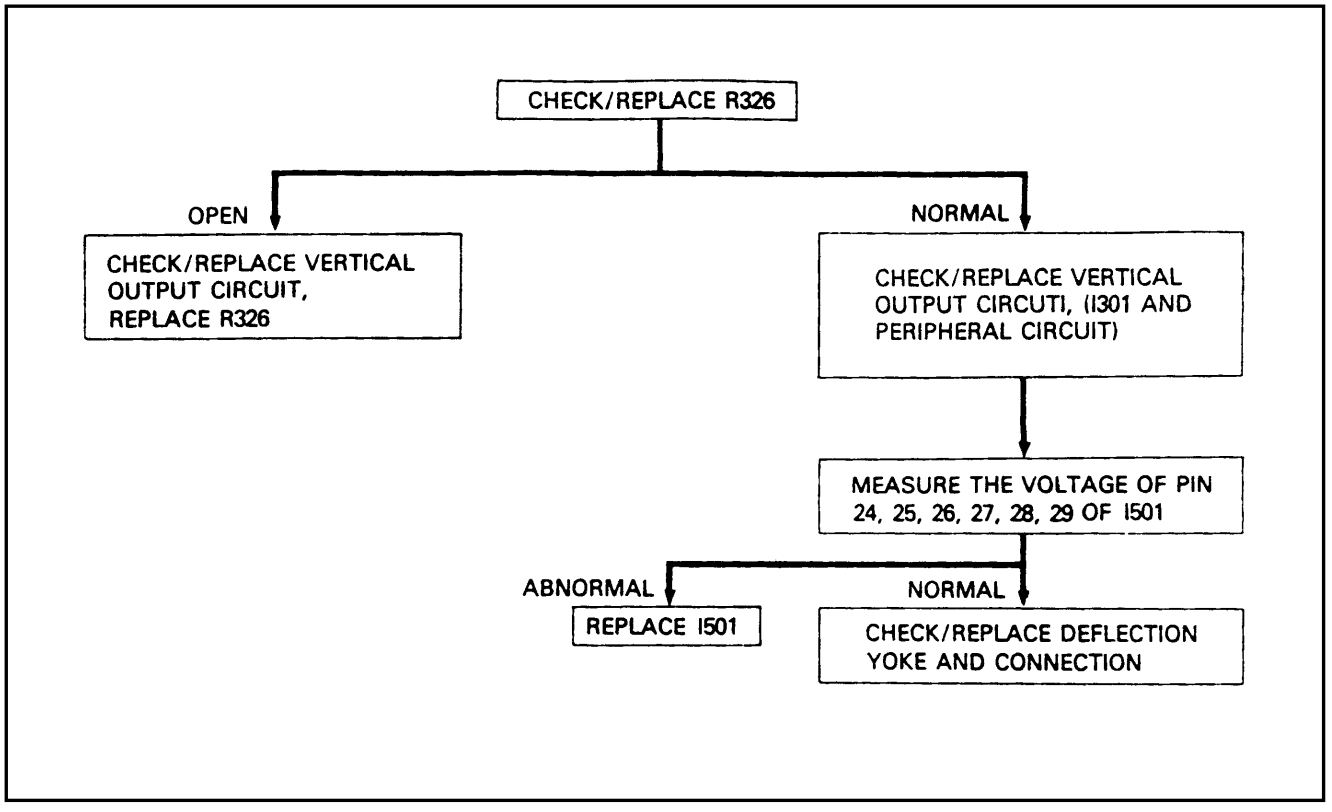
6. NO COLOR



7. SPECIFIC TINTED COLOR



8. NO VERTICAL SCAN (ONE HORIZ. LINE RASTER)



9. OUT OF VERTICAL SYNC. AND HORIZ. SYNC

CHECK REPLACE SYNC SEPARATION CIRCUIT AND I501

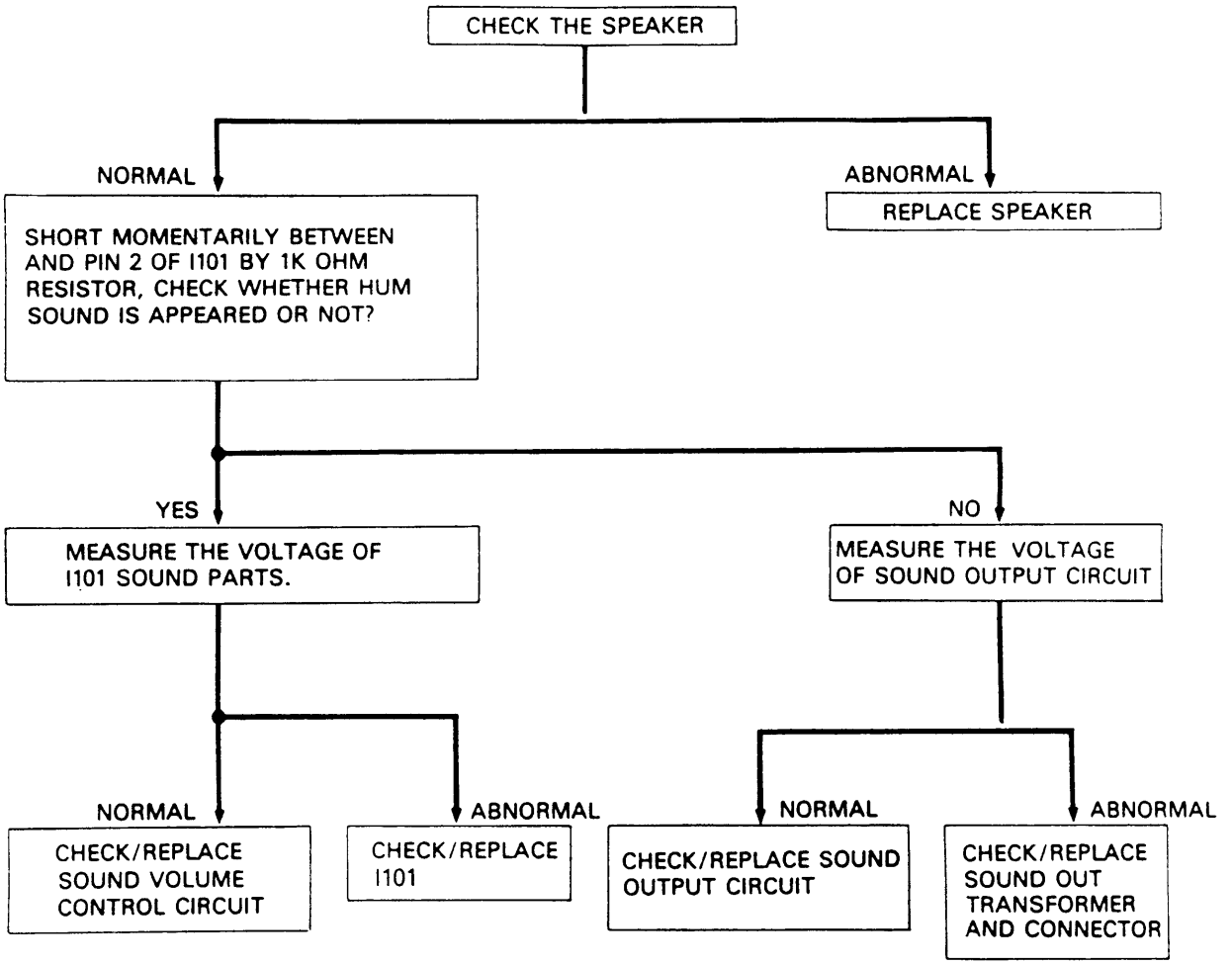
10. OUT OF VERTICAL SYNC

CHECK/REPLACE VERTICAL OSC. PARTS OF I501

11. OUT OF HORIZONTAL SYNC

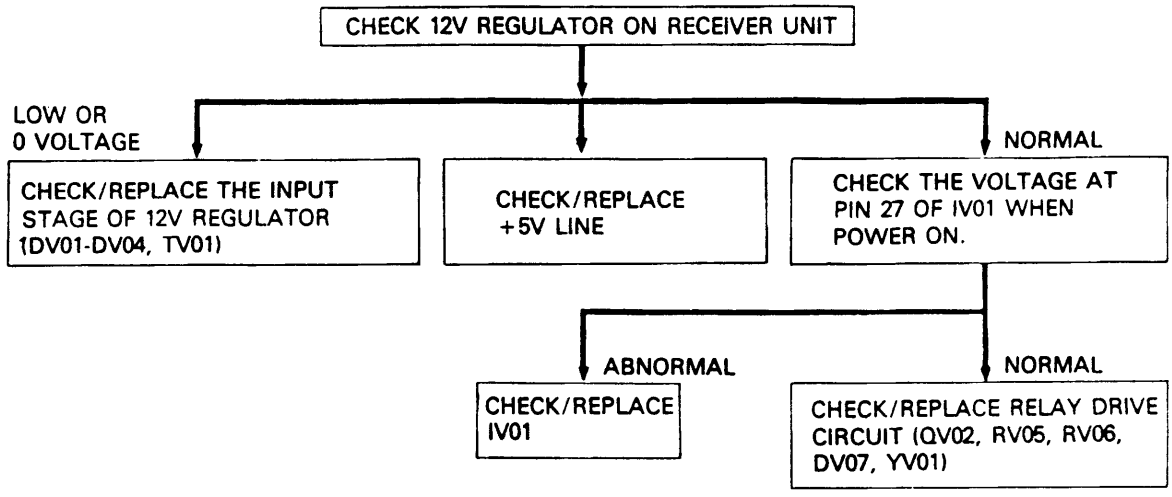
CHECK/REPLACE HORIZ. OSC PARTS OF I501, AFC CIRCUIT

12. NO SOUND

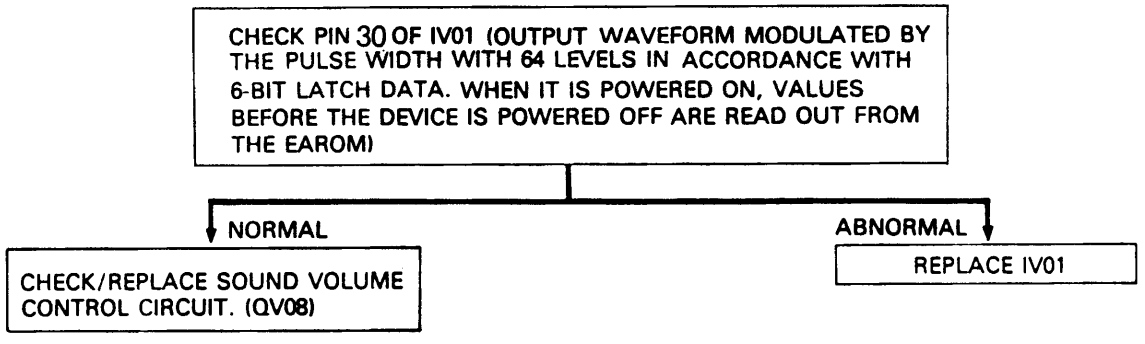

CHECK THE SPEAKER
NORMAL
ABNORMAL
REPLACE SPEAKER
SHORT MOMENTARILY BETWEEN AND PIN 2 OF I101 BY 1K OHM RESISTOR, CHECK WHETHER HUM SOUND IS APPEARED OR NOT?
YES
NO
MEASURE THE VOLTAGE OF I101 SOUND PARTS.
MEASURE THE VOLTAGE OF SOUND OUTPUT CIRCUIT
NORMAL
ABNORMAL
NORMAL
ABNORMAL
CHECK/REPLACE SOUND VOLUME CONTROL CIRCUIT
CHECK/REPLACE I101
CHECK/REPLACE SOUND OUTPUT CIRCUIT
CHECK/REPLACE SOUND OUT TRANSFORMER AND CONNECTOR

13. RECEIVER UNIT OPERATION

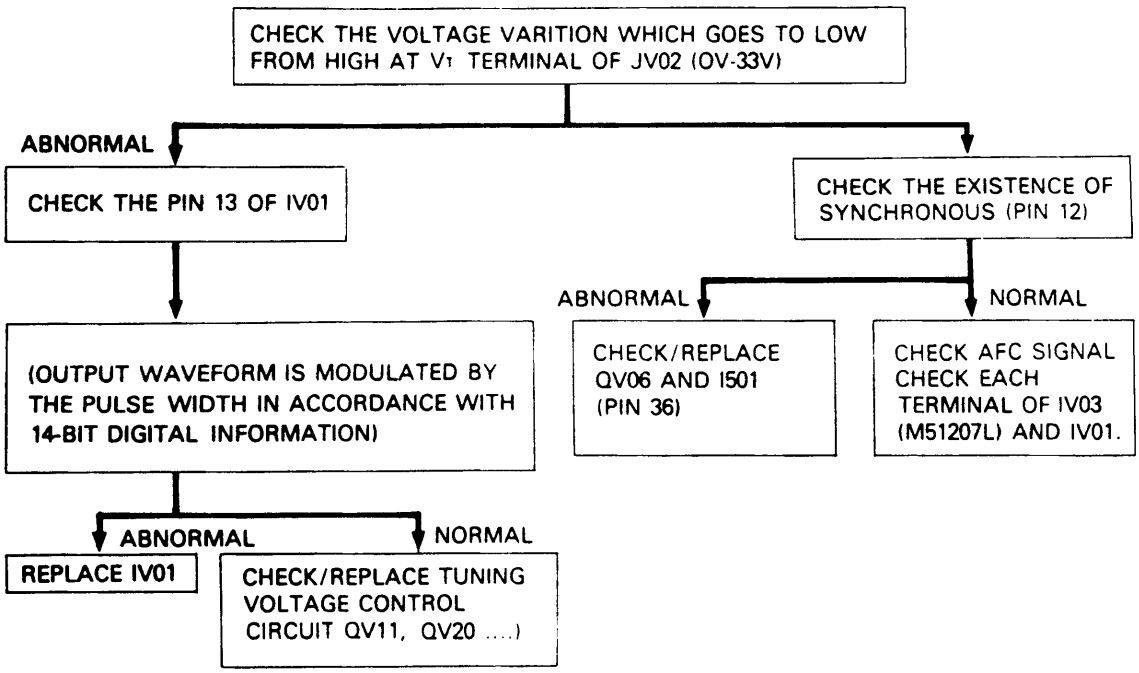
1) NO RASTER



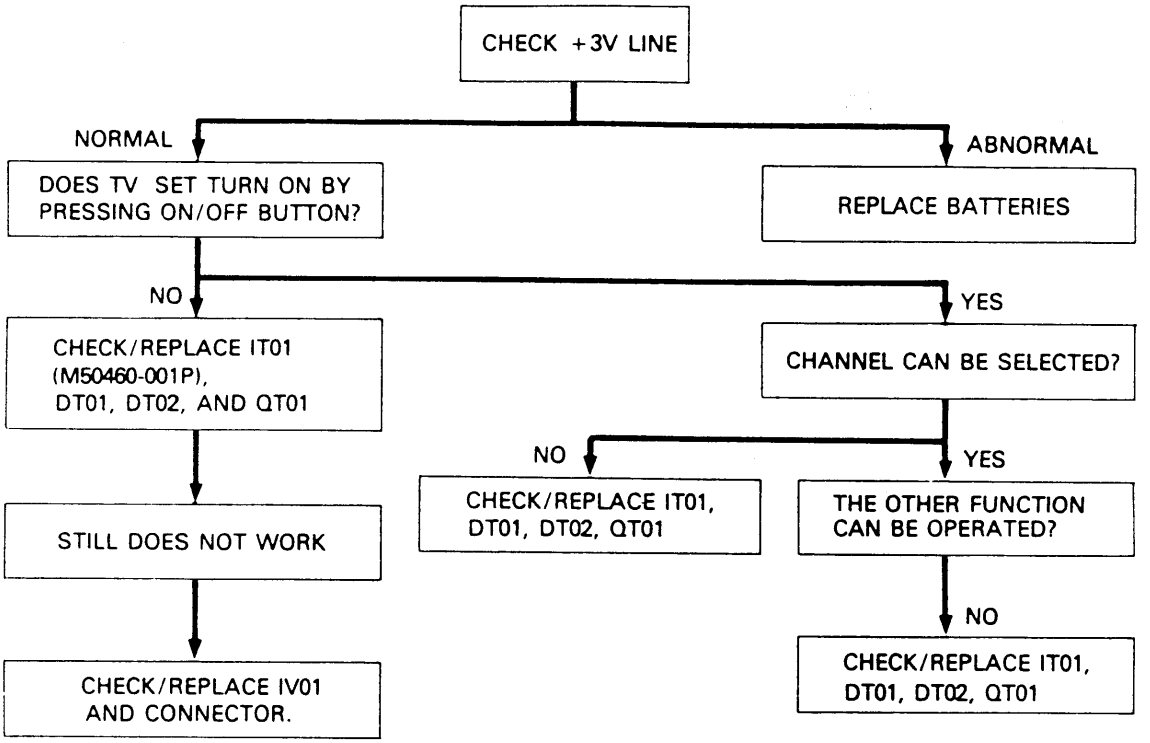
2) NO SOUND



3) NO AUTOMATIC SEARCH OPERATION



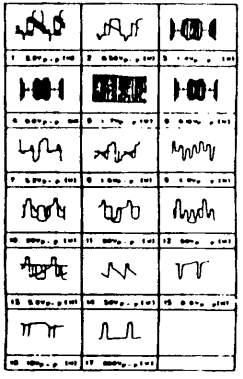
14. REMOTE CONTROL DOES NOT WORK



SAFETY CAUTION

BEFORE SERVICING THIS CHASSIS IT IS IMPORTANT THAT THE SERVICE TECHNICIAN READ AND FOLLOW THE "X-RAY RADIATION PRECAUTION," "SAFETY PRECAUTION" AND "PRODUCT SAFETY NOTICE" IN THIS SERVICE MANUAL.

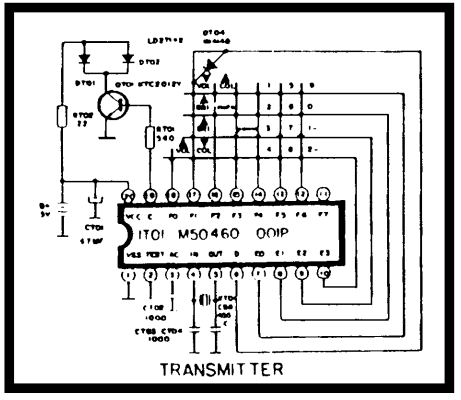
1. WAVEFORMS TAKEN WHERE SHOWN FROM A STANDARD COLOR BAR GENERATOR
2. ○ INDICATES WAVEFORM CHECK POINTS

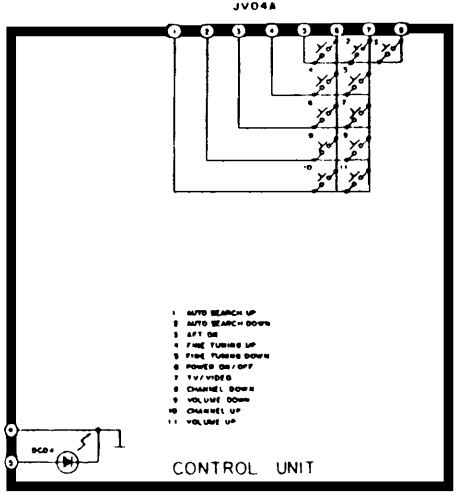


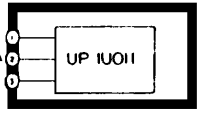
NOTES

1. RESISTANCE VALUES ARE IN OHMS K=1000Ω M=1,000,000Ω
2. CAPACITANCE VALUES 1.0 AND ABOVE ARE IN μF UNLESS OTHERWISE INDICATED
3. INDUCTOR VALUES IN μH UNLESS OTHERWISE INDICATED
4. VOLTAGES ARE MEASURED FROM CHASSIS GROUND TO POINT INDICATED WITH A "VTVM" WHILE RECEIVING A COLOR BAR SIGNAL WITH ALL CONTROLS SET TO THE MAXIMUM POSITION FOR A NOMINAL LINE VOLTAGE 220V~50HZ.
5. SINCE THE CIRCUIT DIAGRAM IS A STANDARD ONE, THE CIRCUIT AND CIRCUIT CONSTANTS MAY BE SUBJECT TO CHANGE FOR IMPROVEMENT WITHOUT ANY NOTICE

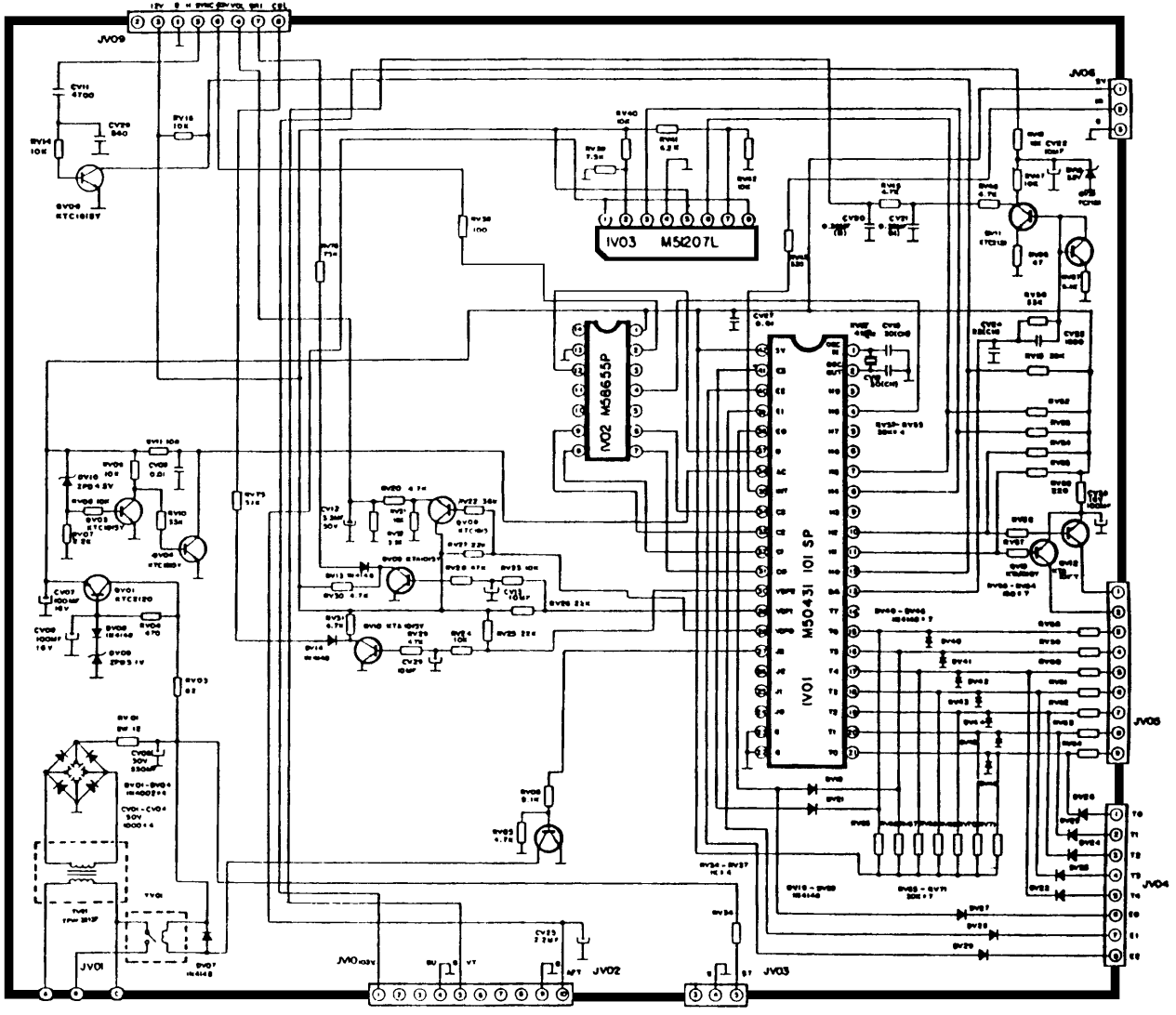
LOCATION NO	14.16 INCH	20 INCH
T 402	DCF-1577	DCF-2077
C 325	0.39 200V	0.47 200V
R 240	24K OHM	18K OHM
R 241	180K OHM	150K OHM
Q 402	2SD 1554	2SD 1555
L 405	L-125	L-102





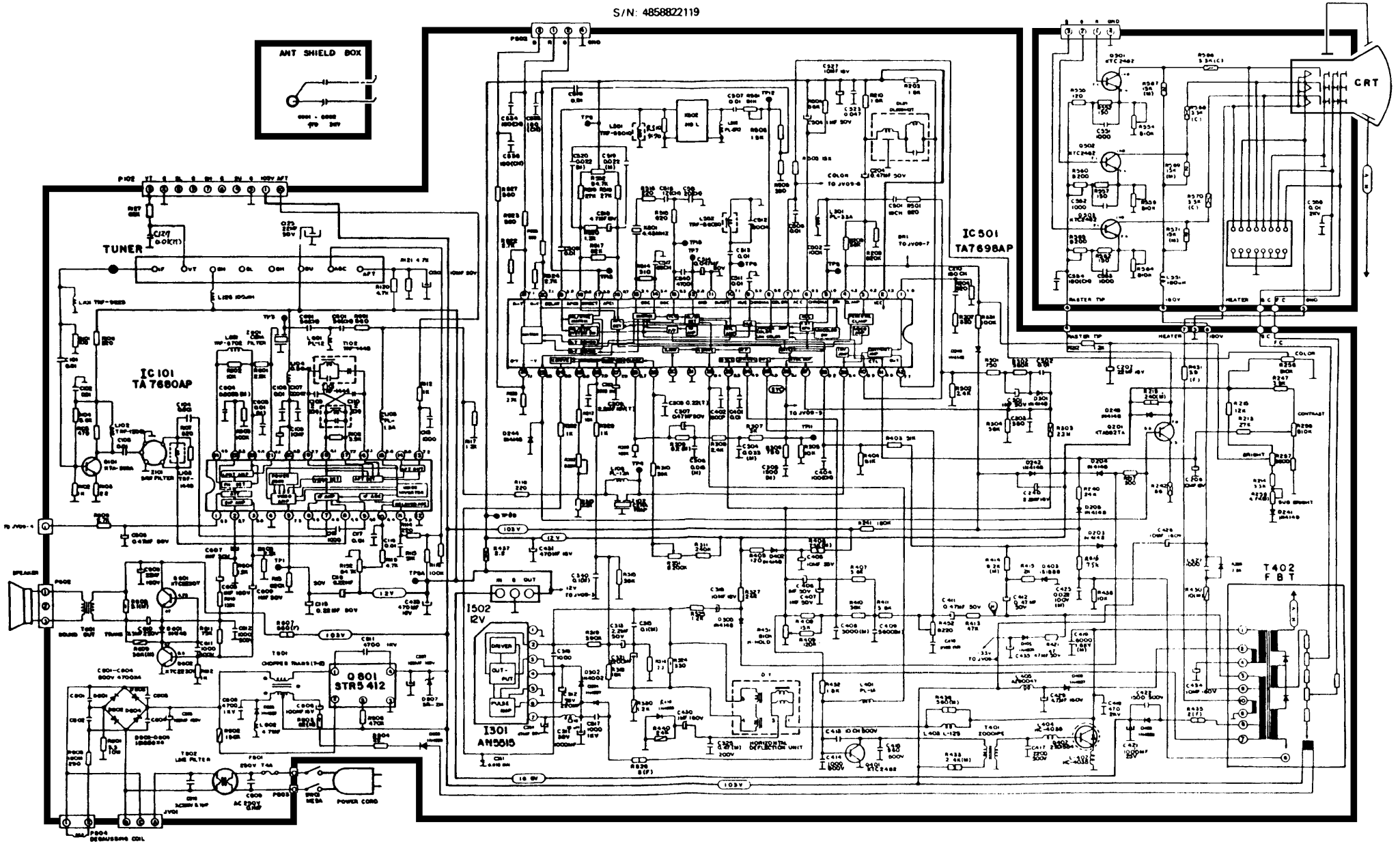






SCHEMATIC DIAGRAM CHASSIS NO:C-43M

S/N: 4858822119



Part Brand	Part Number	Part Description---------	Circuit Reference
DIOD	1N4936	DIODE	D405,6,7 & 10
DIOD	1N4937	DIODE 1N4937	D304
DIOD	1N5397	Diode 1N5397	D403D,801D,2D,3D,4D
IC	AN5515	Ic Tv Vert. Amp p215	I301
IC	DBL2002	ic	
IC	DHR38N	IC	
IC	M50431101SP	ic tuner TV14rc	IV01
IC	M58655P	IC	IV02
IC	SFC7812EC	ic 12v reg	I501
IC	STR5412	IC HN14-13013-1140/1	Q801
IC	TA7698AP	ic	I501
IC	UPC574J	upc574j	DV18
IC	LM393N	Lm393n	IV03
TRAN	2SD1426	vs2sd1426//1e	Q402
TRAN	2SD1554	Alt TRAN 2SD1426	Q402
TRAN	KTA1015Y	KTA1015y	QV9,10,12,13
TRAN	KTA562TMY	KTA562TM-Y(AUTO)	Q201
TRAN	KTC1815Y	KTC1815Y	QV03,04
TRAN	KTC1959Y	q201 ktc1959 trans	QV11,20
TRAN	KTC2120Y	ktc2120y trans	QV01,11,20
TRAN	KTC2230AY	KTC2120Y	Q601,2
TRAN	KTC2482	transistor tv14rc	Q401,501,502,503
TRAN	KTC388ATM	Transistor	Q101
TELR	005315020901	Button touch	
TELR	005410129820	Knob stand-by	
TELR	005415020250	Cabinet	1
TELR	005415020471	Handle Cabinet	5
TELR	005415020571	Holder lamp-1	41
TELR	005415020841	Button-push CH	29
TELR	005415020851	Button-Push Power	29
TELR	005415020861	Button Push Volume	29
TELR	005415021311	Reta LED	40
TELR	005415022960	Retainer Back	2
TELR	005415110801	Door	26
TELR	005415120171	Main PCB Retainer	33
TELR	005415220931	Trans Ant Matching	24
TELR	005451025080	CRT Rubber	6
TELR	005455023140	Label Control Panel	53
TELR	005461142911	Deco Ch Glass	28
TELR	005716020451	Cover Back	50
TELR	005905119791	Cover SW	
TELR	013000004670	Shield Cover	
TELR	013000004680	Shield Plate	
TELR	013010004660	Shield Case	
TELR	013488004531	Spring SWPA	32
TELR	013920008020	Bracket FBT	
TELR	013988060450	Spring Ground.Wire	
TELR	014002106001	Pin B Term Pres	
TELR	014112106001	Pin B Term	
TELR	014410090400	Terminal Fuse Clip	
TELR	015012208150	Screw Met.M3X8 YSB	49
TELR	015611207290	Screw Tin Plated	

Part Brand	Part Number	Part Description---------	Circuit Reference
TELR	015611210290	Screw Tin Plated	
TELR	015611213290	Screw Tin Plated	
TELR	015611216390	Screw Tin plated	
TELR	015611916290	Screw Tin Plated	
TELR	015641813390	Screw Tin Plated	
TELR	015641816390	Screw 3.9X16 YSB	
TELR	015841295290	Screw 2.9X9.5 RYSB	
TELR	015901230501	Screw CRT FIX 5*30	8
TELR	016002225150	Nut M3 BS	
TELR	017108045110	Galvanized Washer	
TELR	030050633211	R Carbon Comp	R566,658,570
TELR	030055630011	R Fusible 3R 1/2W %5	R326
TELR	030105620901	R Fusible 2R 1W %5	R435
TELR	030105656101	R Fusible 560R 1W %5	R607
TELR	030205639901	R Fusible 3.9R 2W %5	R431
TELR	032100633901	R Cement(longtype)	R801
TELR	034710541821	Positor	R805
TELR	037720007831	Filter sfe 6.0m	Z601
TELR	037730007831	Filter tps 6.0m	Z102
TELR	037750007841	Filter Saw F1035	Z101
TELR	037940008021	Filter Line LF-3138	T801
TELR	048773809001	LED DKLR114E RED	DC04
TELR	049010000581	Coil	DL01
TELR	049010000601	Coil Chroma delay	X502
TELR	049030000061	Crystal 4.433619mhz	X501
TELR	049040040001	crystal 4mhz	XV01
TELR	065001007330	instruction manual	
TELR	065156007420	Label Cover Back	
TELR	065320007440	Label Trans.Remoc.	
TELR	067600002161	Ant Loop	
TELR	075020800011	PCB CRT Socket	
TELR	081002124901	SW Push on/off	
TELR	081501211601	Switch SW tact	
TELR	399000000101	Ant Shield Box	24
TELR	602200003311	Trans Sound Out	T601
TELR	602300003321	Trans H-Drive	T401
TELR	602800003301	Trans smps t-2	T801
TELR	602940001451	Trans Power	TV01
TELR	604200000721	FBT DCF-1577A LOPTX	T401
TELR	608380002331	Coil Bead hc-4035	
TELR	608380002341	Choke trf9247(4.7uh)	L802
TELR	608380002351	Choketrf9225(0.55uh)	L101
TELR	608380002371	Choke trf1201B(0.97uh)	L102
TELR	608380003481	Coil Peaking 0.56uh	L104
TELR	608380003521	Coil Peaking 8.2uh	L502
TELR	608580002021	Coil Degaussing	9
TELR	608780002401	Coil Filter trf5501q	L551
TELR	608780003821	Coil H-Linearity	L403
TELR	608880002381	Coil Demod trf5605q(4.406m	L552
TELR	608880003841	Coil Aft.trf1445U(39.5mhz)	T102
TELR	608880003851	Coil Pif trf1444U(39.5mhz)	T101
TELR	608880003861	Coil Trap trf1448U	L103

Goodmans 1401R Parts list

Part Brand	Part Number	Part Description---------	Circuit Reference
TELR	608880003871	Coil Sif trf6702	L651
TELR	608980000071	Coil Peaking 1uh	L401
TELR	608980002461	Coil 1.3uh	L105
TELR	608980002471	Coil 180uh	L551
TELR	608980003691	Coil Peak 12uh	L106,601
TELR	608980003731	Coil Filter trf3703v(6mh)	
TELR	608980003741	Coil Peak 10uh	L310
TELR	608980003751	Coil Peak 100uh	L126
TELR	609330001011	SW Relay	YV01
TELR	609330001021	Display LED ddr204a	DC04
TELR	610006312041	Speaker	
TELR	611110022011	R Semi-Fixed 200r	R560,565
TELR	612413000001	VR Rotary Block	
TELR	616800000391	Tuner VaractorVTS-uk	
TELR	621003051041	100n 250v AC	C810
TELR	631070001001	Handset Remocon	
TELR	075020800011	CRT Base assy Block	
TELR	841112010903	Main PCB assy Block	
TELR	841150010903	Receiver assy Block	
TELR	841160010900	IR receiver assy Block	
TELR	841120010903	Control-on/off assy Block	
TELR	841130010903	Display assy Block	

EXPLODED VIEW

1) 14 INCH

