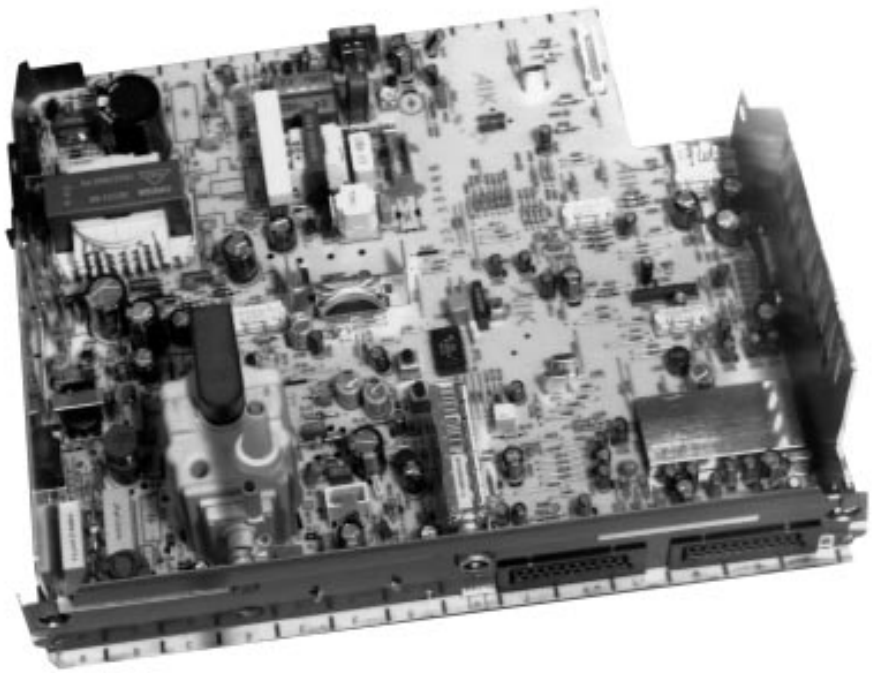
THOMSON MULTI MEDIA

Brandt FERGUSON SABA TELEFUNKEN THOMSON

APPLIED STUDY OF TELEVISION SETS
ICC17 RACK



Code : 350 683 60 - 09/98 - APPLIED STUDY OF TELEVISION SETS - ICC17 RACK

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MANAGEMENT

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THE CONTROLS

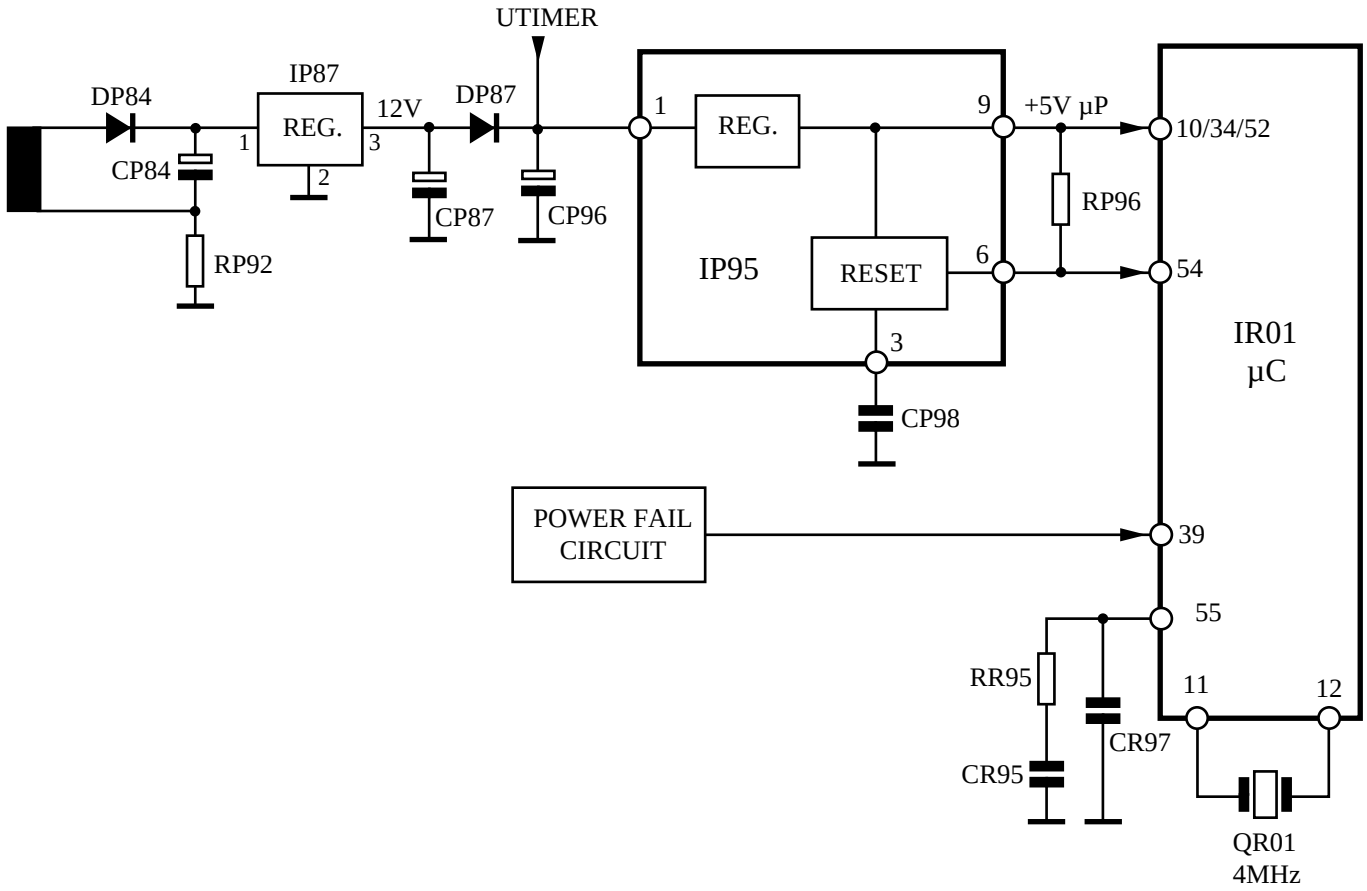
MEMORIES AND IIC BUS

MENU AND TELETEXT

TIMER/ON

OTHER PINS ON THE IR01

FAILURE CODES


UTIMER
IP87
DP84
REG.
12V
DP87
1
3
2
CP84
RP92
CP87
CP96
1
REG.
9
+5V µP
10/34/52
RP96
IP95
RESET
6
54
3
IR01
µC
CP98
POWER FAIL
CIRCUIT
39
55
RR95
11
12
CR97
CR95
QR01
4MHz

POWER SUPPLY AND FUNCTIONS SIGNALS FOR IR01

POWER SUPPLY

The power supply for the IR01 micro-controller, pins 10, 34 and 52, originates in TIMER mode, from regulator IP87 (MC7812) and the 5V regulator incorporated in IP95. In ON mode, it is supplied with power from the UTIMER voltage via the 5V regulator incorporated in IP95.

CLOCK

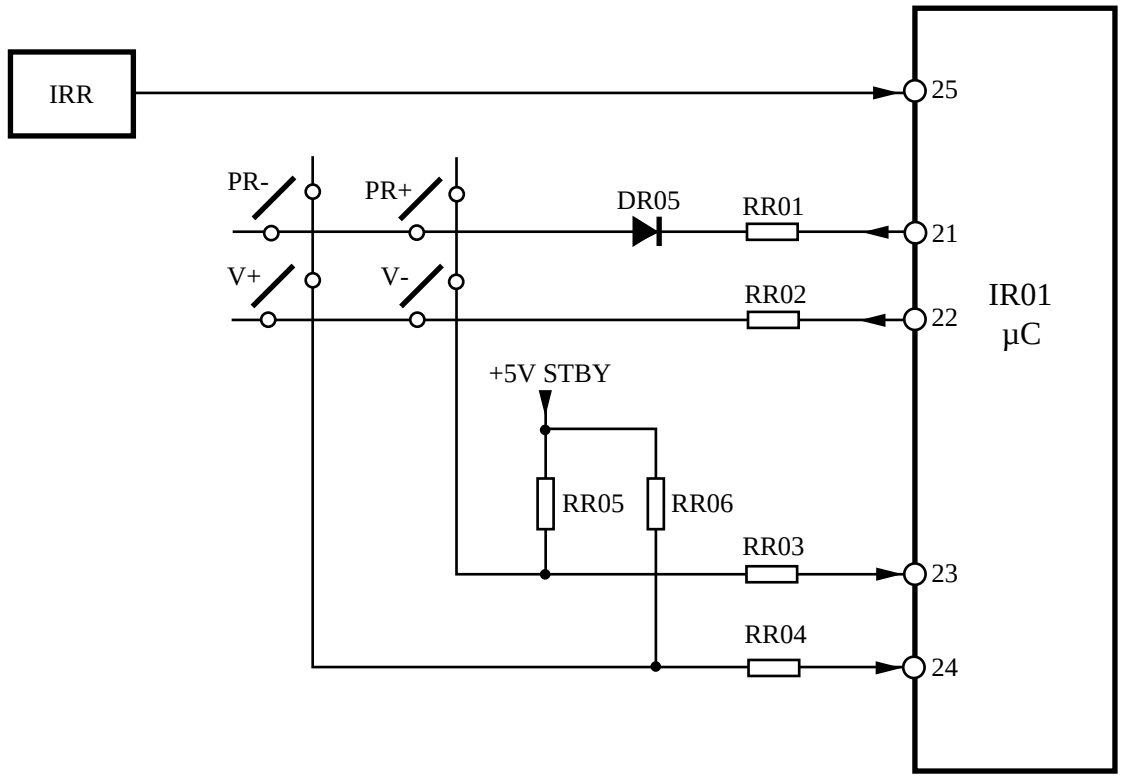
A 22 MHz VCO/PLL assembly internal to IR01 manages the micro-controller. The quartz, QR01, 4 MHz, is used as a reference for the PLL. The components RR95, CR95 and CR97 constitute the loop filter for the PLL.

RESET

CP98, pin 3 of IP95, is the reset capacitor. When the voltage at 9 of IP95 reaches 5V and after a delay of a few milliseconds issued by CP98, pin 6 of IP 95 changes from 0 to 5V. Pin 54 of the IR01 receives the RESET information.

DETECTION OF MAINS POWER CUT

This circuit is analysed in the power supply chapter.


IRR
25
PR-
PR+
DR05
RR01
21
V+
V-
RR02
22
IR01
µC
+5V STBY
RR05
RR06
RR03
23
RR04
24

THE CONTROLS

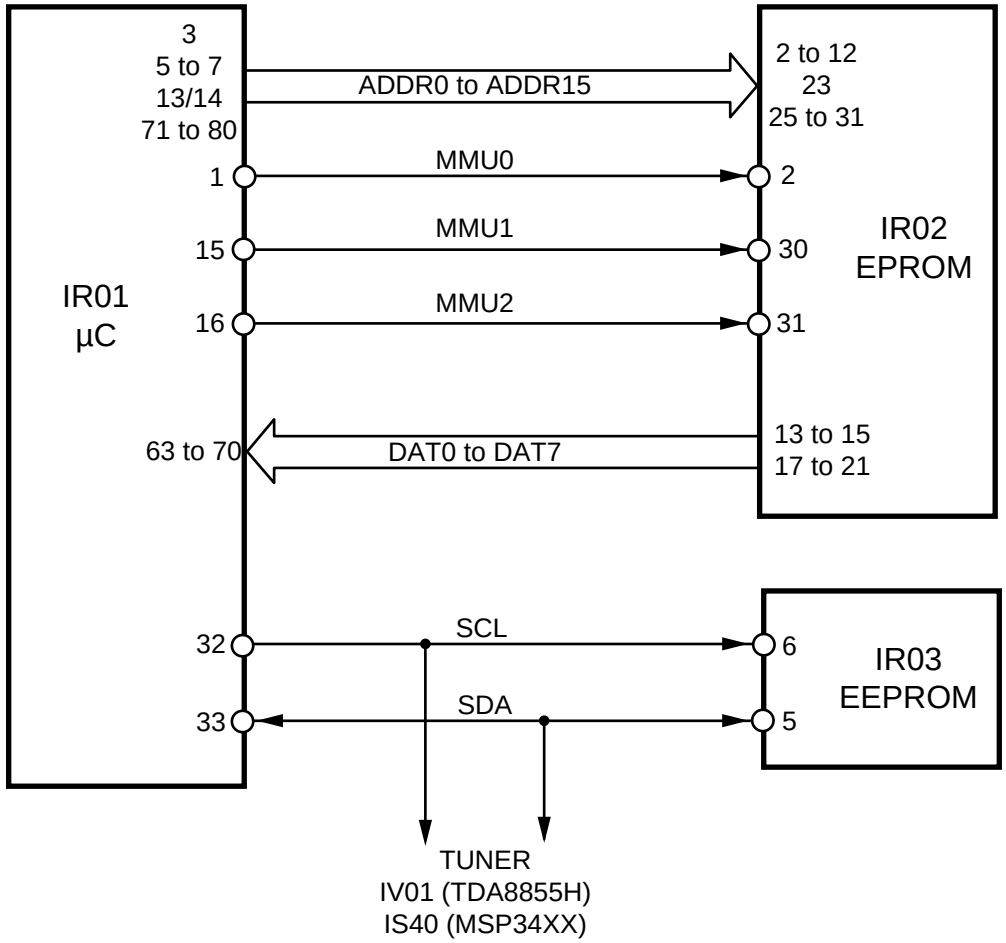
THE KEYBOARD

The keyboard has 4 keys. It is arranged in a line/column matrix. Pins 23 and 24 are the function inputs and are at 5V when inactive. Pins 21 and 22 are scanning outputs, they are at 0V when inactive. When a key is pressed, a scanning signal of period approaching 12 ms is generated, either at output 21 (PR keys) or output 22 (V keys).

THE REMOTE CONTROL

The remote control function codes (12 bits) are received at 25 of IR01. These are composed of:
- 4 address bits
- 1 call bit
- 7 function bits, which are defined by the key pressed.

These codes are repeated every 80 ms.


IR01
µC
3
5 to 7
13/14
71 to 80
ADDR0 to ADDR15
2 to 12
23
25 to 31
IR02
EPROM
1
MMU0
2
15
MMU1
30
16
MMU2
31
63 to 70
DAT0 to DAT7
13 to 15
17 to 21
32
SCL
6
IR03
EEPROM
33
SDA
5
TUNER
IV01 (TDA8855H)
IS40 (MSP34XX)

MEMORIES AND IIC BUS

IR02 MEMORY

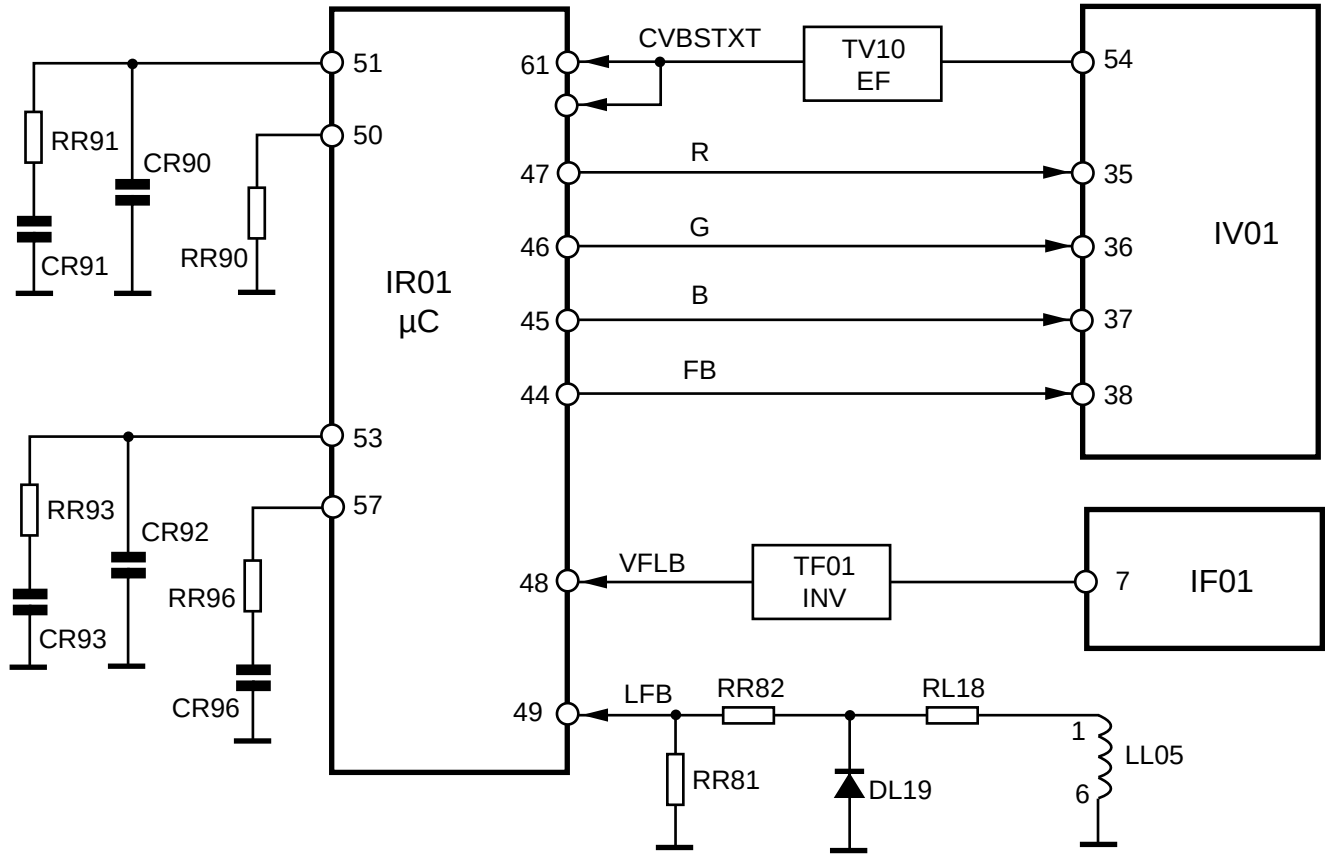
IR02 is an EPROM memory with a capacity of 512 Kbytes or 4 Mbits. It is the software memory of the IR01 and for the default values of service mode. The lines MMU0 to MMU2 are an extension of the address bus.

IR03 MEMORY

IR03 is an EEPROM memory, capacity 1 Kbyte or 8 Kbits. It contains the coefficients of service mode, the user adjustments (brightness, contrast, etc.) the synthonised TV channels and if applicable, stand-by command, etc.

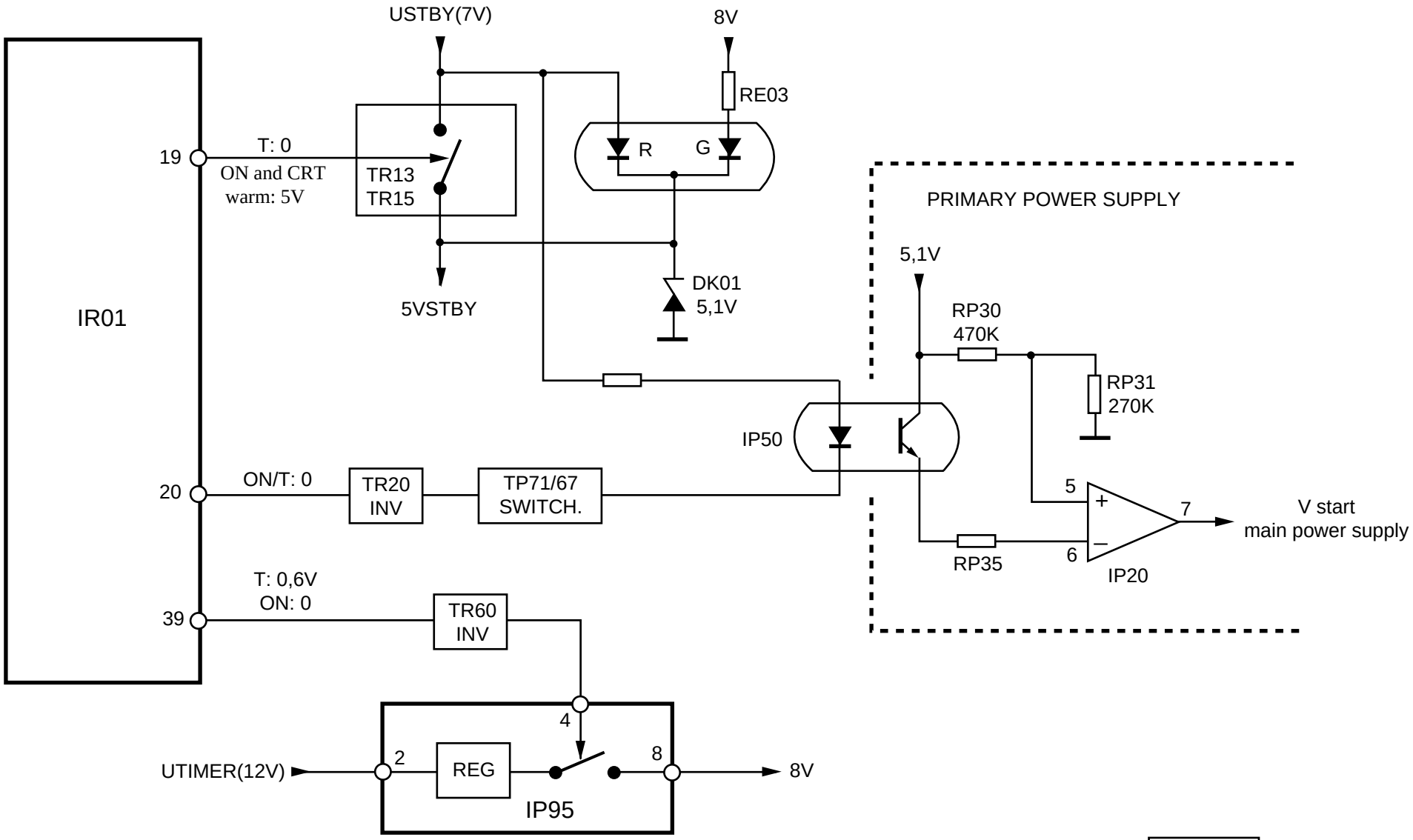
IIC BUS

The IIC bus is charged by pull-up resistors linked to the 5V DC. It is enabled in TIMER and ON modes. It dialogues with or controls the IR03 EEPROM, the tuner, the IF/video/IV01 time bases and the audio processing circuit IS40.
Its operating frequency is in the order of 80 KHz.
Acknowledgement of receipt of IR03, IV01 and IS40 are taken into account by IR01. In the case of absence of the latter, IR01 issues a failure code.


IR01
µC
51
50
53
57
61
47
46
45
44
48
49
RR91
CR90
CR91
RR90
RR93
CR92
CR93
RR96
CR96
CVBSTXT
TV10
EF
54
R
G
B
FB
35
36
37
38
IV01
VFLB
TF01
INV
7
IF01
LFB
RR82
RL18
RR81
DL19
1
6
LL05

MENU AND TELETEXT

IR01 manages menus and teletext. It incorporates a TDSRAM memory of 8Kbits for storing teletext data.
The teletext data are extracted from the CVBSTXT signal entering at 61 of IR01. The wide screen signalling data (line 23) are extracted form the CVBSTXT signal entering at 60 of IR01.
The RVBs (0.7 V dc) and rapid switching (2.5 V dc) are available on pins 47 to 44 of IR01
The VFLB signals (5V dc frame return) and LFB signals (5V dc line return) fix the position of the overlays.
The R/C components connected at 50/51 of the IR01 manage the VCO/PLL assembly for the WSS.
The R/C components connected at 53 of the IR01 are used as the frequency multiplier for the display.
The R/C components connected at 57 of IR01 are used for the teletext data sampling clock.


USTBY(7V)
8V
RE03
R
G
19
T: 0
ON and CRT
warm: 5V
TR13
TR15
5VSTBY
DK01
5,1V
IR01
PRIMARY POWER SUPPLY
5,1V
RP30
470K
RP31
270K
IP50
20
ON/T: 0
TR20
INV
TP71/67
SWITCH.
5
7
V start
main power supply
RP35
6
IP20
T: 0,6V
ON: 0
39
TR60
INV
4
2
REG
8
UTIMER(12V)
8V
IP95

TIMER/ON

TIMER

The level at the IR01 pins and the status of circuits are as follows:

- Pin 19: 0
  This generates opening of switch TR13/15, power supply for the red LED from USTBY and power supply for the infra-red receiver and keyboard from the 5V STBY.

- Pin 20: 0
  This generates the bringing into service of the main power supply, thanks to stopping saturation of the photo-sensor IP50 and the IP20 comparator voltages (pin 5/6: approx. 1.8V and pin 7: 6V)
  The management µC is supplied with power.

- Pin 39: 0.6V
  This causes absence of the 8V (IP95 internal switch is open) and consequently, non supply of IV01.

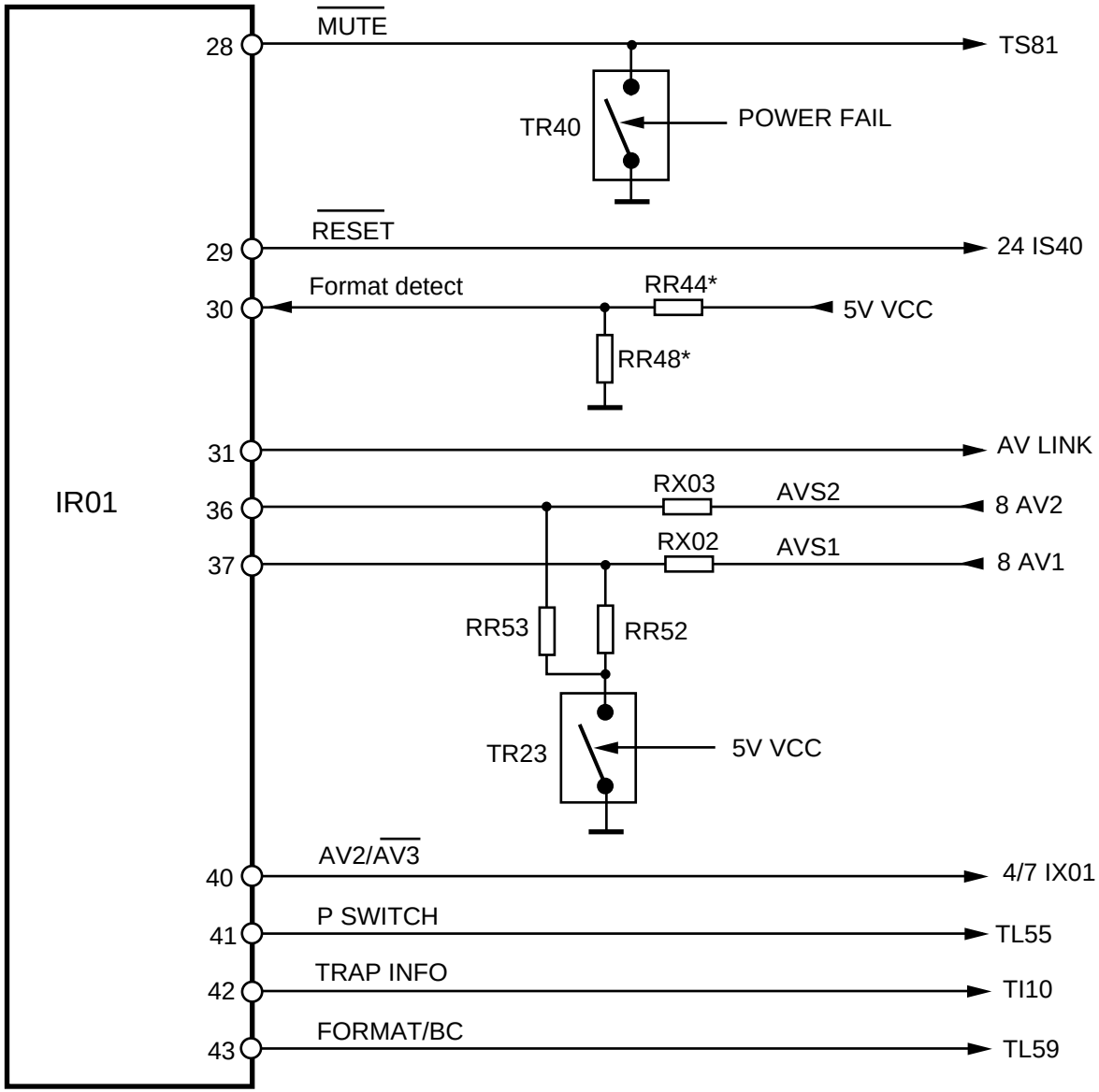
ON

The level at the IR01 pins and the status of circuits are as follows:

- Pin 19: 5V when the tube is warm
  This causes closing of the switch TR 13/15 and extinguishing of the red LED.

- Pin 20: 0
  This generates the bringing into service of the main power supply, thanks to stopping saturation of the photo-sensor IP50 and the IP20 comparator voltages (pin 5/6: approx. 1.8V and pin 7: 6V)
  The management µC is supplied with power.

- Pin 39: 0
  This generates the 8V, power supply of the green LED and of IV01.


IR01
28
MUTE
TS81
TR40
POWER FAIL
29
RESET
24 IS40
30
Format detect
RR44*
5V VCC
RR48*
31
AV LINK
36
RX03
AVS2
8 AV2
37
RX02
AVS1
8 AV1
RR53
RR52
TR23
5V VCC
40
AV2/AV3
4/7 IX01
41
P SWITCH
TL55
42
TRAP INFO
TI10
43
FORMAT/BC
TL59

OTHER PINS ON THE IR01

- PIN 28 (MUTE)
Enabled at low level, this controls the audio mute during:
  - changing of programmes
  - searching for a transmitter
  - cutting off the sound (silence key)
  - switching on the TV set when the tube is not warm
  - switching off the TV set
  - the stand-by and timer functions.
    The transistor TR40 saturated on stand-by (power fail = 5V) completes the mute on stand-by.

- PIN 29 (RESET)
Enabled at low level for 5 ms, this resets the audio processing circuit MSP34XX. It acts when the TV is switched on and each time the TV channel is changed.

- PIN 30 (FORMAT DETECT)
By cabling the resistor RR44 or the resistor RR48, this indicates to IR01 the type of tube with which the TV set is equipped.
RR44 cabled, tube 4/3, 5V at 30 of IR01
RR48 cabled, tube 16/9, 0V at 30 of IR01
This pin is analysed by IR01 in TIMER mode.

- PIN 31 (AV LINK)
Currently, this pin is not used.

- PINS 36/37 (AVS2.AVS1)
This receives slow switching from pins 8 of the SCART connectors AV2 and AV1. The range of voltages for these inputs are as follows:
  - AV 16/9: 0.96V < V < 1.44V
  - AV 4/3: 2.96 < V < 3.44V

The stand-by output of the TV set can be realised by AVS2/AVS1 via RR52 or RR53 and DR23. The transistor TR23, blocked during stand-by, allows this command. The transistor TR23 saturated when on, brings into service the resistive dividers.

- PIN 40 (AV3)
This allows taking into account signals from AV2 or AV3 (control of the integrated switching circuit IX01)
AV2: 5V; AV3: 0V.

- PIN 41 (P SWITCH)
This allows changing format of the image by modifying the value of the S capacitor.
16/9 - ZOOM1: 0; 4.3 centred: 5V

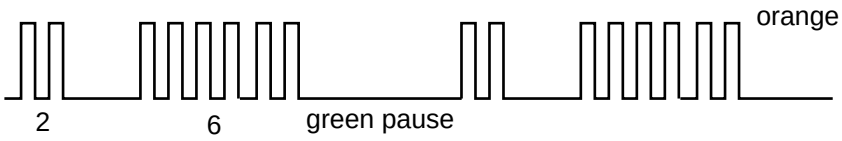
- PIN 42 (TRAP INFO)
This allows putting into service a 31.9 MHz rejector in BG (rejection of adjacent channel)
BG: 0; OTHERS: 5V

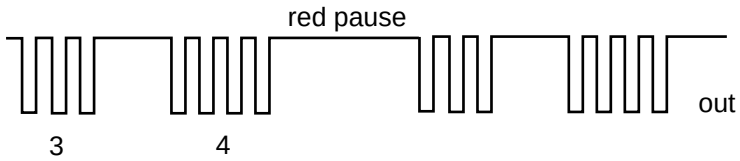
- PIN 43 (FORMAT/BC)
This supplies a PWM signal of 5 V dc with period 186 µs. Via TL59/TL02, it adjusts the voltage of beam current limitation (BCL) depending on the image format.

FAILURE CODES

The failure codes are displayed by the red LED. They can be visualised solely if the management *C is operating.
A maximum of 81 codes can be displayed (11 to 99). These codes are comprised of 2 figures separated by a pause of 0.7 seconds. A period of 1.7 seconds separates two failure codes. The failure codes are repeated a minimum of 4 times.

SEQUENCE OF SIGNALS AT RED LED TERMINALS





LIST OF FAILURE CODES

CODES	DEFECTS
14	ACR TDA8855H
15	ACR MSP34XX
21	DATA IIC GROUNDED
23	CLOCK IIC GROUNDED
25	5V SWITCHING ABSENT
26	NO INFORMATION ON TUBE HOT AFTER 25 SEC
27	PROTECTION ENABLED 3 TIMES
28	VERTICAL GUARD EXCESSIVE
34	ACR NVM 24C08
36	NVM ADDRESS NOT FOUND
37	NMI LEVEL INCORRECT (HALT)
41	IIC BUS BLOCKED

POWER SUPPLY

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INTRODUCTION

PRESENTATION

STAND-BY POWER SUPPLY

STAND-BY MODE AND QUITTING STAND-BY

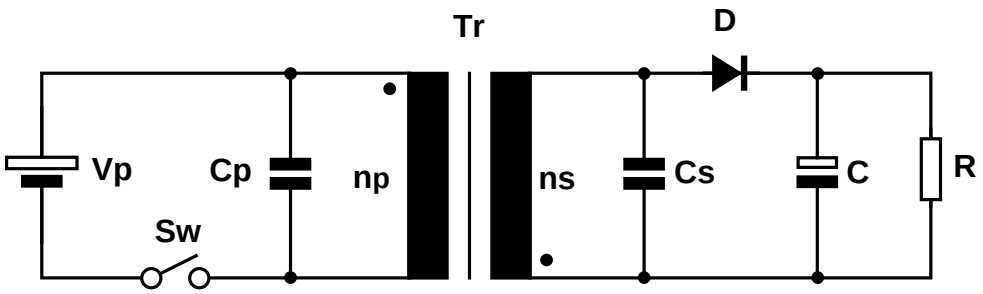
MAIN POWER SUPPLY

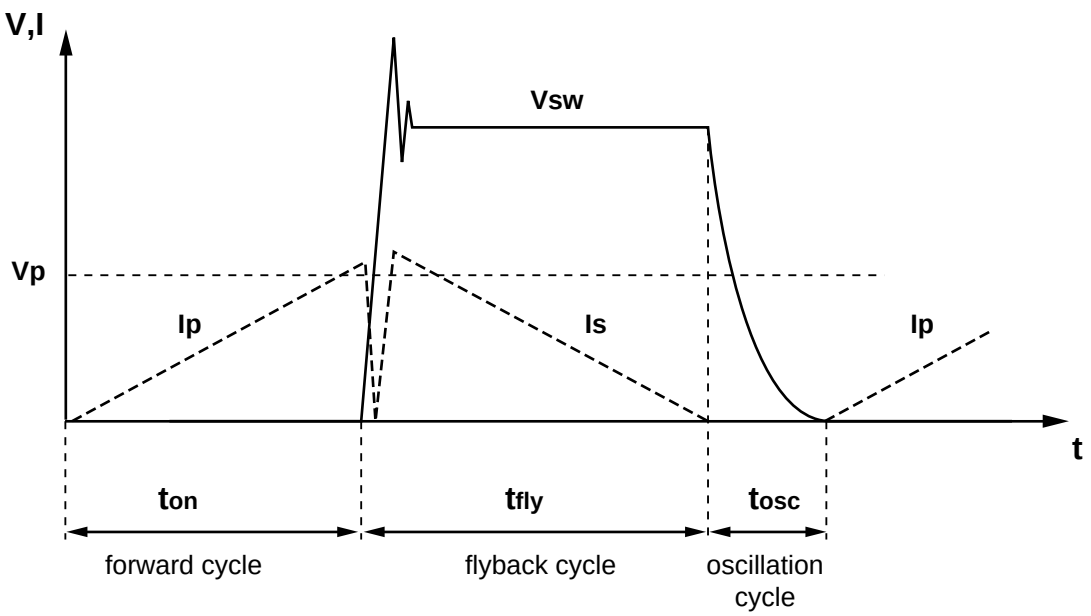
SECONDARIES

SECONDARY SUPPLIES

TUBE DEMAGNETISATION CIRCUIT

MAINS POWER CUT DETECTION CIRCUIT


Tr
D
Vp
Cp
np
ns
Cs
C
R
Sw

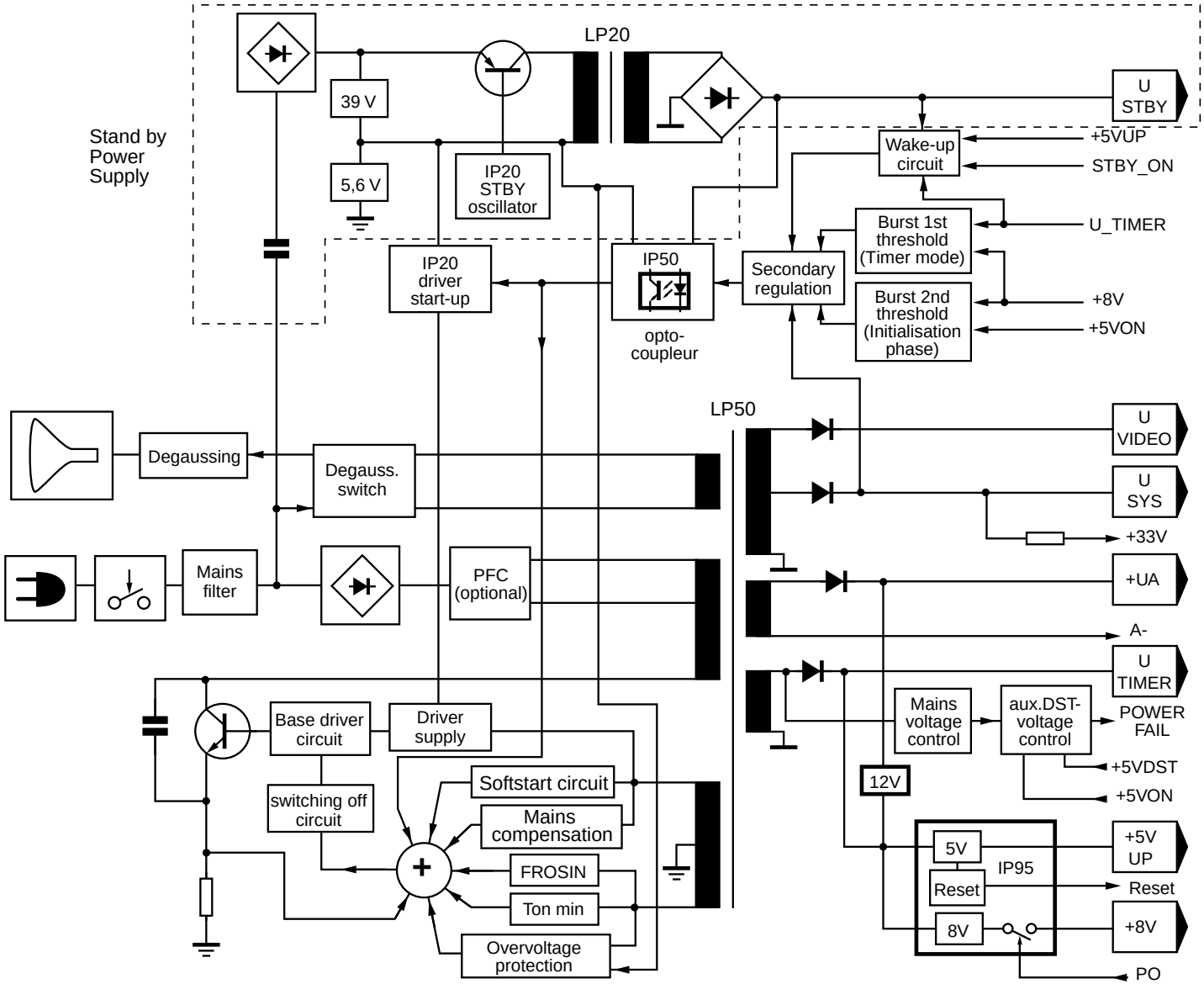

V,I
Vsw
Vp
Ip
Is
Ip
t
ton
tfly
tosc
forward cycle
flyback cycle
oscillation cycle

INTRODUCTION

The ICC17 rack satisfies 2 needs:
- supplying a large range of power to ensure maximum power of 47 watts for the image and 2 * 10 watts rms for the audio (respectively 35 watts and 2 * 5 watts rms for the TX92F).
- to display low consumption in stand-by (=< 0.5 watts)

This is the FROSIN concept (FRee Oscillation Safe INtelligent) coupled with a two pole transistor which was selected, associated with a separate stand-by power supply.
A mode intermediary to stand-by and the normal regimen exists : "Timer" mode. This corresponds to the stand-by mode for previous racks, supplying the micro-controller (approx. 3 watts).

The FROSIN principle reduces voltage at the de-coupling collector when switching and is here reinforced by the ZVS concept (Zero Voltage Switching) ensuring that voltage at the collector is almost zero during switching.
The disadvantage of this is high voltage at the collector of the de-coupling transistor during the restitution phase, requiring a collector/transmitter component with a high maximum voltage (Vces > 1500 volts), a characteristic linked to LOW GAIN.



SYNOPTIQUE DES ALIMENTATIONS

PRESENTATION

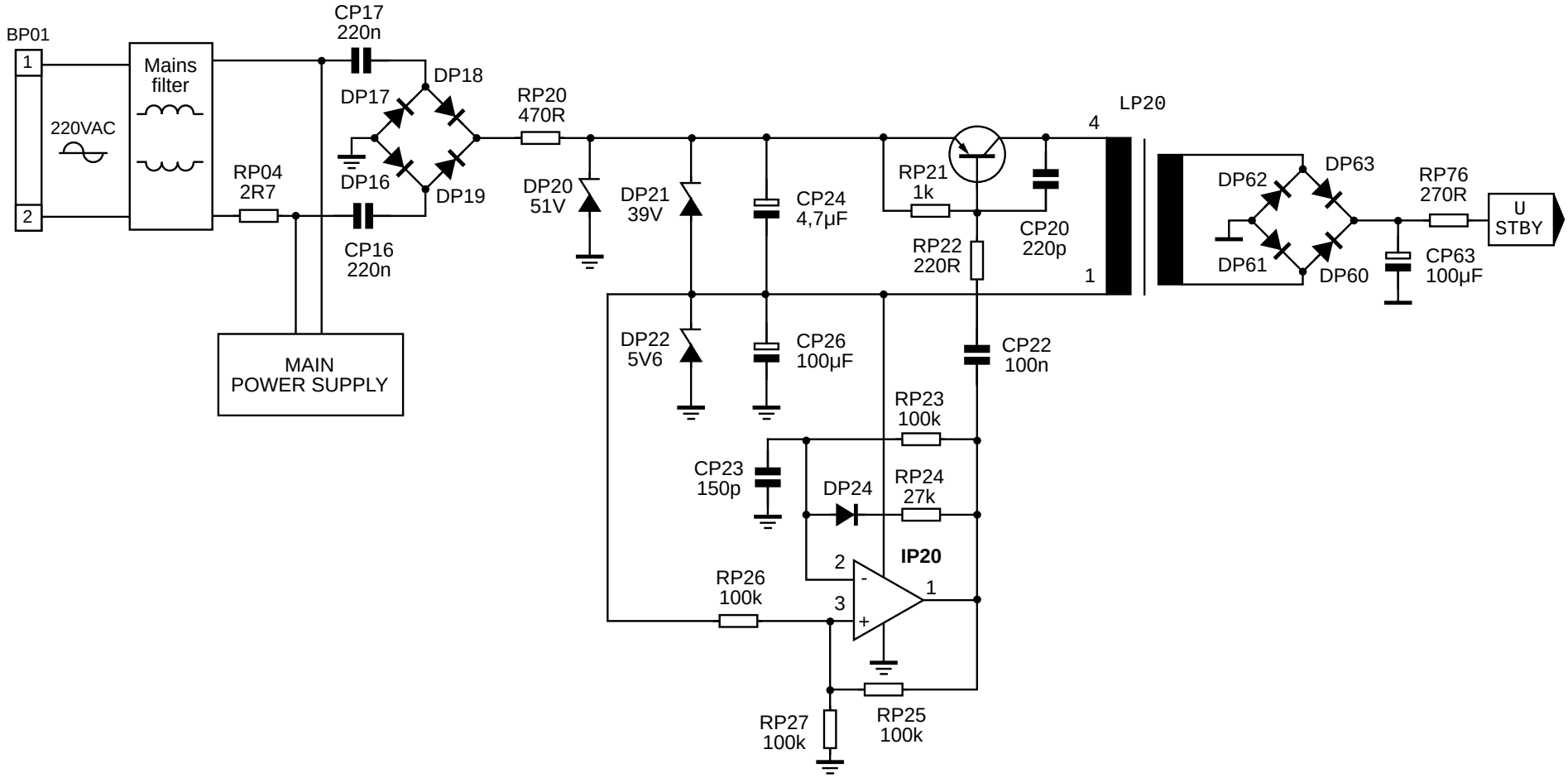
The stand-by power supply supplies, after rectification, 2 voltages stabilised by zeners which supply respectively, the transformer primary (39 volts) and the oscillator (5.6 volts).
The secondary supply provides the non-regulated USTBY voltage of approx. 7 volts.
The switch-on stage enabled by the STBY-ON data starts up the main power supply via the secondary regulation stage and the opto-coupler.

The control stage is first of all supplied by the "driver start-up" circuit and is subsequently self-supplied.
The splitter transistor base is controlled by the blocking circuit via a new base driver stage.
Conduction time is linked to the combination of various circuits:
- regulation (opto-coupler)
- soft start-up and mains compensation (forward mode)
- FROSIN, minimum sound and detection of over voltage (flyback mode)
- current limitation (transmitter resistance)

A triac switches demagnetisation of the tube, whereas an optional power factor correction circuit is provided for.
Secondary regulation stabilises the secondary voltages in TIMER mode (1st threshold), during start-up (2nd threshold) and in the normal regimen (USYS stabilising).

Four secondary windings supply respectively:
- the Uvideo voltage
- the USYS voltage for scanning
- power supply for the audio stage + UA
- 12 Volts UTIMER

Supplied in TIMER mode by + UA via IP87 and by U TIMER in normal regimen, circuit IP95 supplies:
- the permanent 5 VUP and reset for management
- 8 volts power supply for the video processor switched by the micro controller via the PO control.



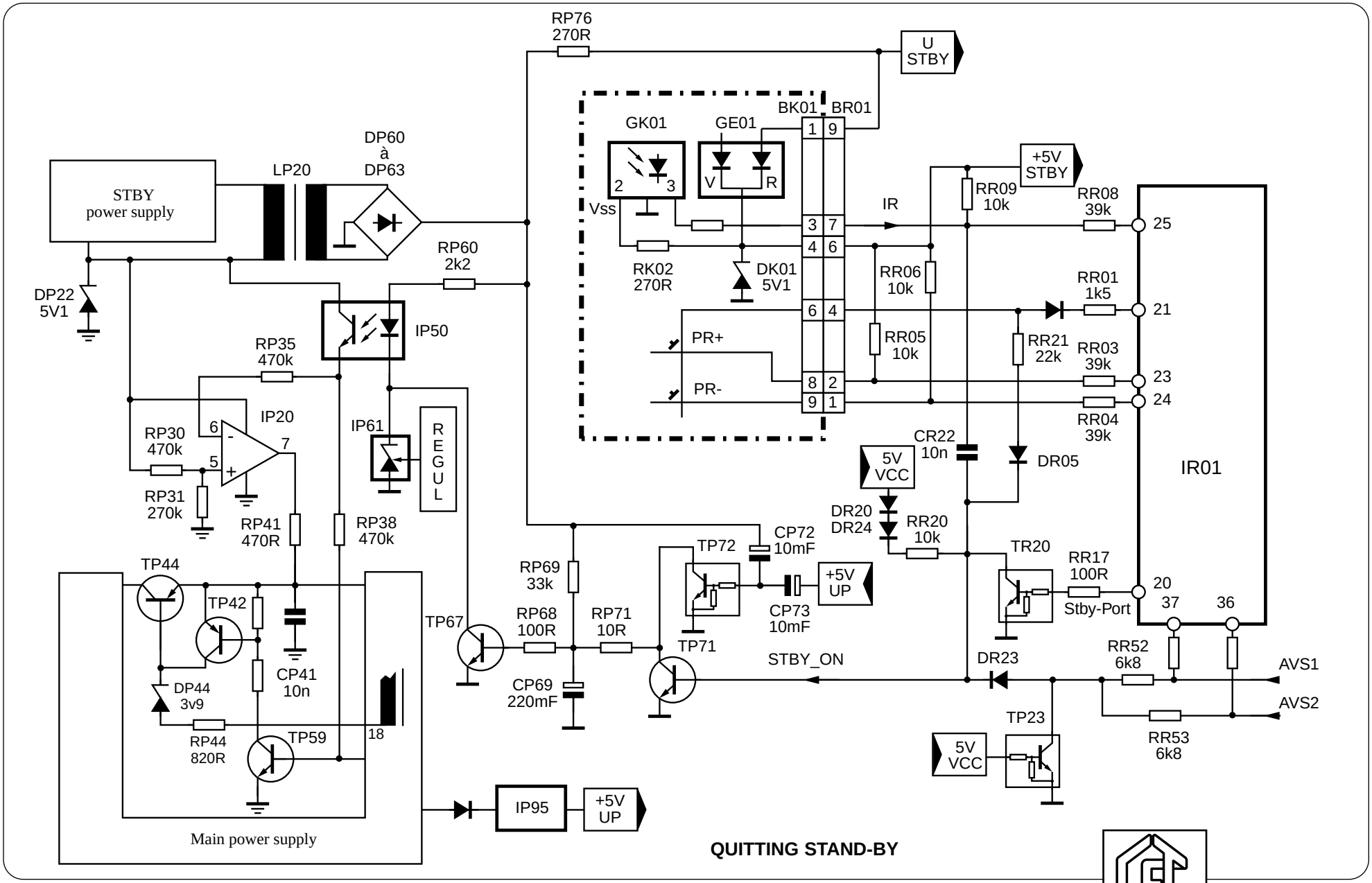
STAND-BY POWER SUPPLY

24

STAND-BY POWER SUPPLY

The bridge rectifier DP16 to DP19 samples the current through capacitors CP16 and CP17.
Two serial zeners DP21 and DP22 stabilise the rectified voltage to supply respectively :
- with 39 volts, the LP20 primary and the TP21 splitter
- with 5V6, the opto-coupler transistor and the oscillator IP20 (pins 1, 2, 3)

This latter is cabled in non stable fashion (F = 65 KHz, T = fl)
The transistor TP21 is saturated during each low level (4 microseconds) via CP22.
At the secondary, the 2 alternating currents are rectified by bridge DP60 to DP63 to obtain USTBY (7 volts). This voltage supplies :
- the opto-coupler diode
- the red LED and the zener diode DK01 (+ 5V STBY)
- the infra red receiver
- the front panel keyboard
- an AV switching detection stage.



QUITTING STAND-BY

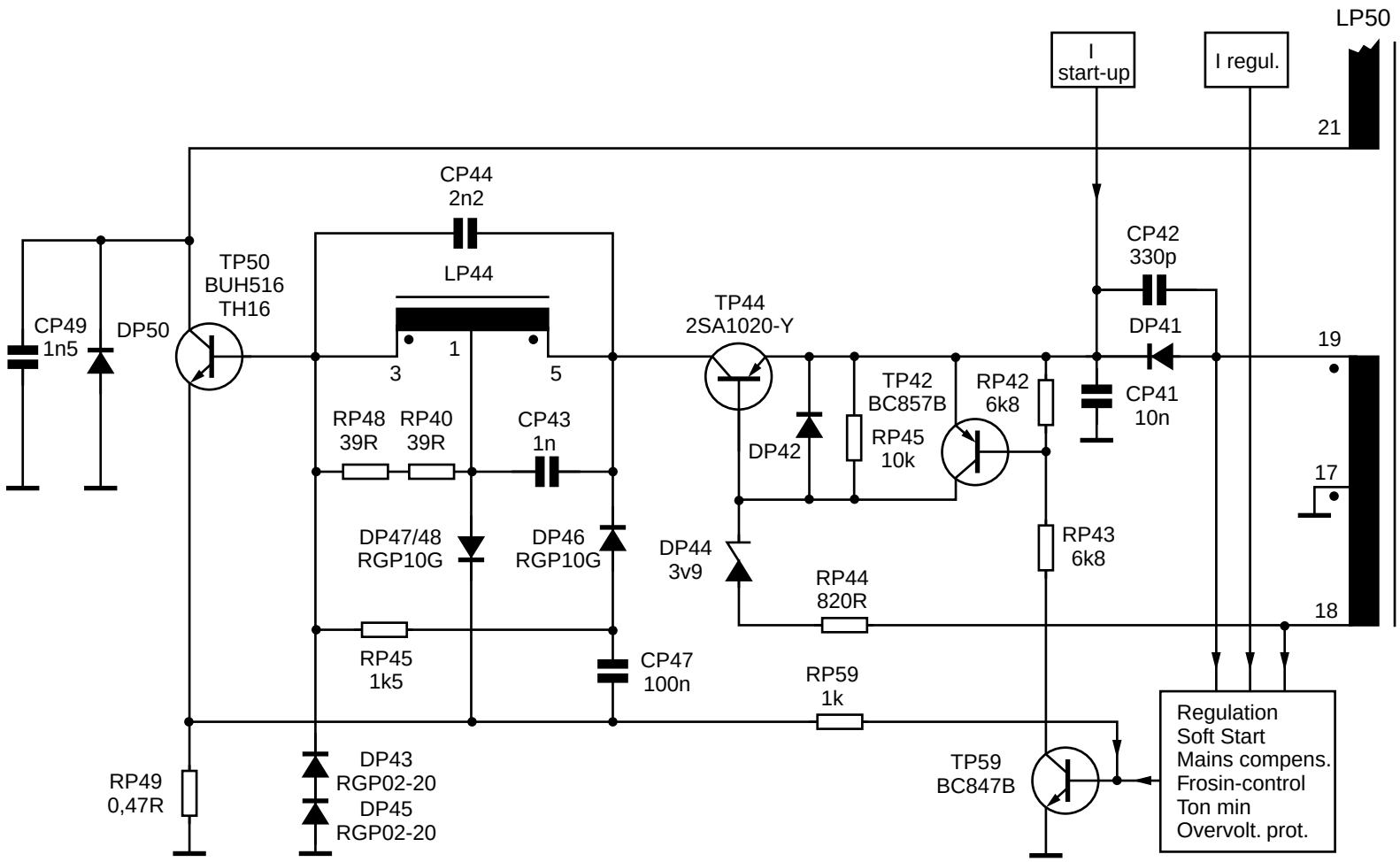
STAND-BY MODE

In stand-by mode, TP 71 and TP72 are blocked (STBY-ON line at 0), CP69 is charged, TP67 is saturated and maximum current passes through the opto-coupler.
At the primary, the regulation currents saturate TP59 via RP38, whereas a high level via RP35 is imposed at the inverse input of IP20, (pin 6), suppressing the start-up power supply (low level on pin 7 of IP20). No current can reach the base of TP50 and the main power supply is inactive.

QUITTING STAND-BY

The STBY-ON line changes to high status in constant or cyclical fashion in the following cases:
- receipt of an infra red signal
- pressing of key PR+ or PR- on the front panel keyboard
- slow switching command AV1 or AV2 (TR23)

TP71 discharges CP69, TP67 is blocked and current in the opto-coupler reduces by action of the serial programmable shunt diode IP61.
At the primary, the regulation current also decreases, the ampliop IP20 (pins 5, 6, 7) switches, supplying by its output at pin 7 (5V6) the capacitor CP41 whereas the base of TP59 is liberated.
When CP41 reaches approx. 4V5, TP44 conducts and supplies current to the base driver stage, thus starting up the main power supply.
The micro controller again forces stand-by via transistor TR20 after 8 seconds if the commands have disappeared in the meantime.



THOMSON MULTI MEDIA

CENTRE DE FORMATION TECHNIQUE

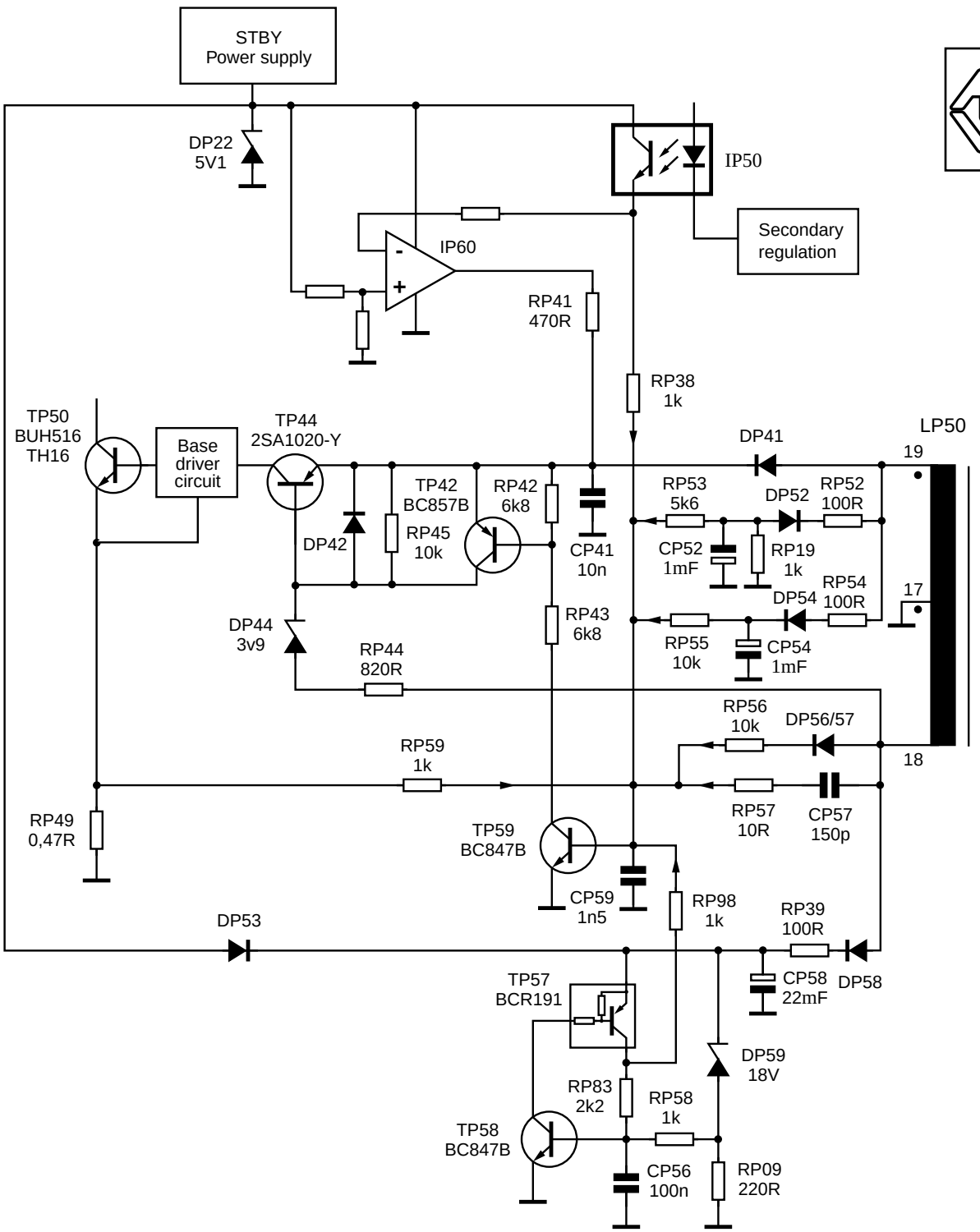
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MAIN POWER SUPPLY

The main power supply is basically composed of two major parts:
- preparation of the base current of TP50 (self supplied: DP41/CP41, switching: TP44, formatting: LP44 and associated components)
- the validation/inhibition circuit for this current: the cut-off circuit (TP59/TP42).

PREPARATION OF BASE CURRENT FOR TP50

The load of the capacitor CP41 generates the base current of TP50. This charge is assured during start-up by IP20, then via the diode DP41.
This current is applied at the base of TP50 by the intermediary of TP44 and LP44 (base driver). TP44 conducts during start-up for CP41 - 4V5 (zener DP44) then when the cut-off circuit is blocked (TP42 no longer short circuits the junction be of TP44)
At the end of the storage cycle, the cut-off circuit (TP42/59) is saturated and blocks transistor TP44. LP44 then becomes a generator and maintains current according to 2 circuits:
- first circuit: from mid point of LP44 via DP47/DP48, through CP47 and returning through the input (pin 5) by DP46. CP47 is then negatively charged in relation to the ground (negative voltage at the base of TP50 during the energy restitution phase)
- second circuit: on account of the fact that the 2 coils of LP44 are in opposite directions, the induced voltage which is generated between points 1 and 3 generates a second current opposite to the first. This starts from the middle of the coil via DP47/DP48 through the junction of TP50 (unloading of the junction)



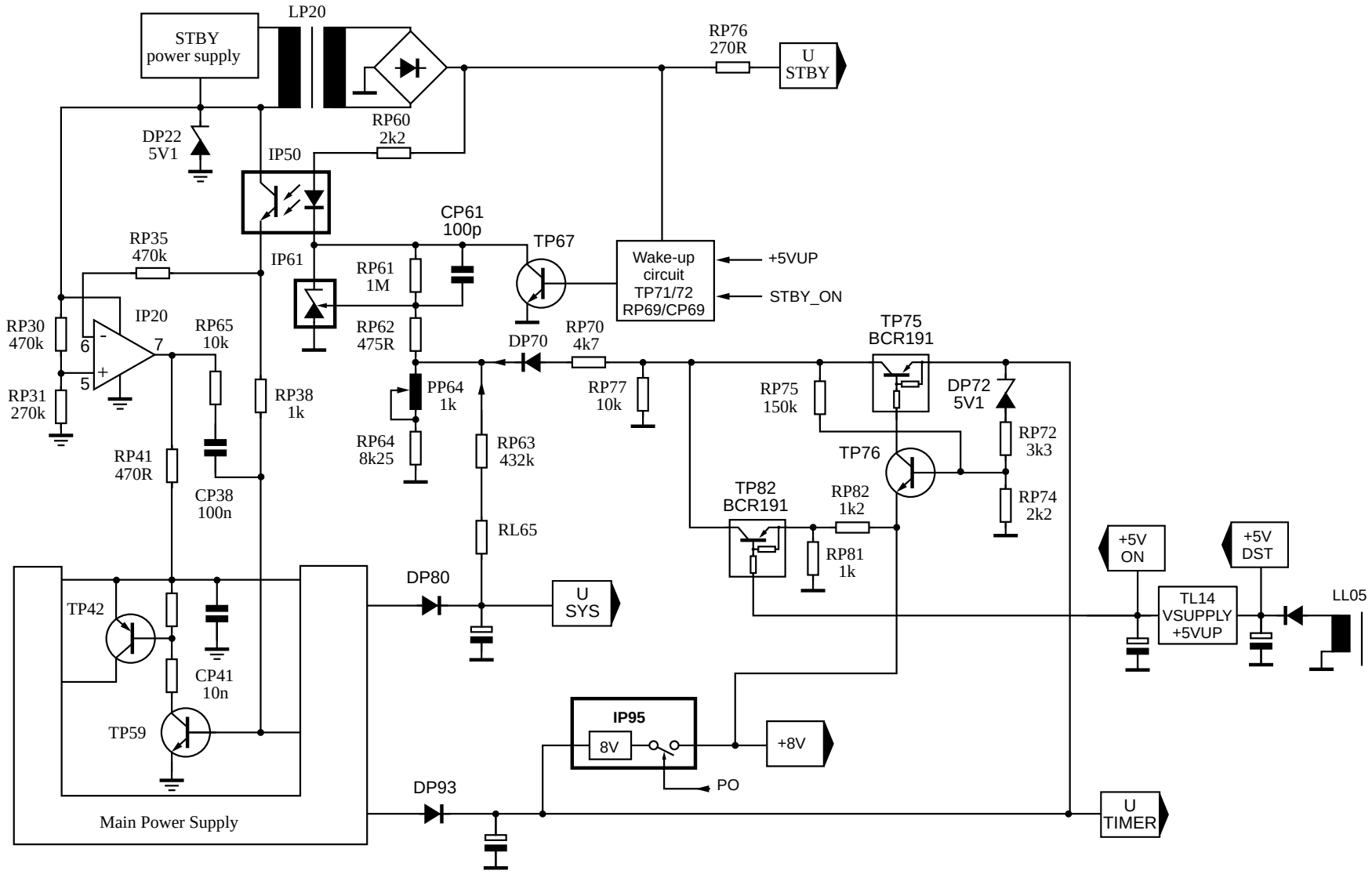
CUT-OFF CIRCUIT

CUT-OFF CIRCUIT

7 data items are applied at the base of TP59 and determine, by the combination of their effects, more or less rapid blocking of TP50:
- regulation (IP50, RP38)
- the principle primary current limit threshold (RP49, RP59)
- soft start-up (DP52, CP52)
- mains compensation (DP54, CP54)
- the FROSIN circuit (DP56/57, RP56)

This circuit ensures, at the end of the restitution cycle, by controlling the saturation current (RP56), a time delay linked to the discharging time of transistors TP59/TP42.
An oscillation phase is also permitted at the TP50 collector allowing saturating this component when the collector voltage is minimal:
- the minimum sound circuit (RP57, RP56)
- protection against over voltage.

An image of the secondary voltages is recreated at the primary by fly-back rectification (pin 18 of LP50, DP58 and CP58). Once this voltage exceeds the 19 volts threshold (zener DP59 + Vbe TP58) the pseudo thyristor assembly TP57/58 is triggered, blocking TP50 by permanent saturation of the cut-off circuit.



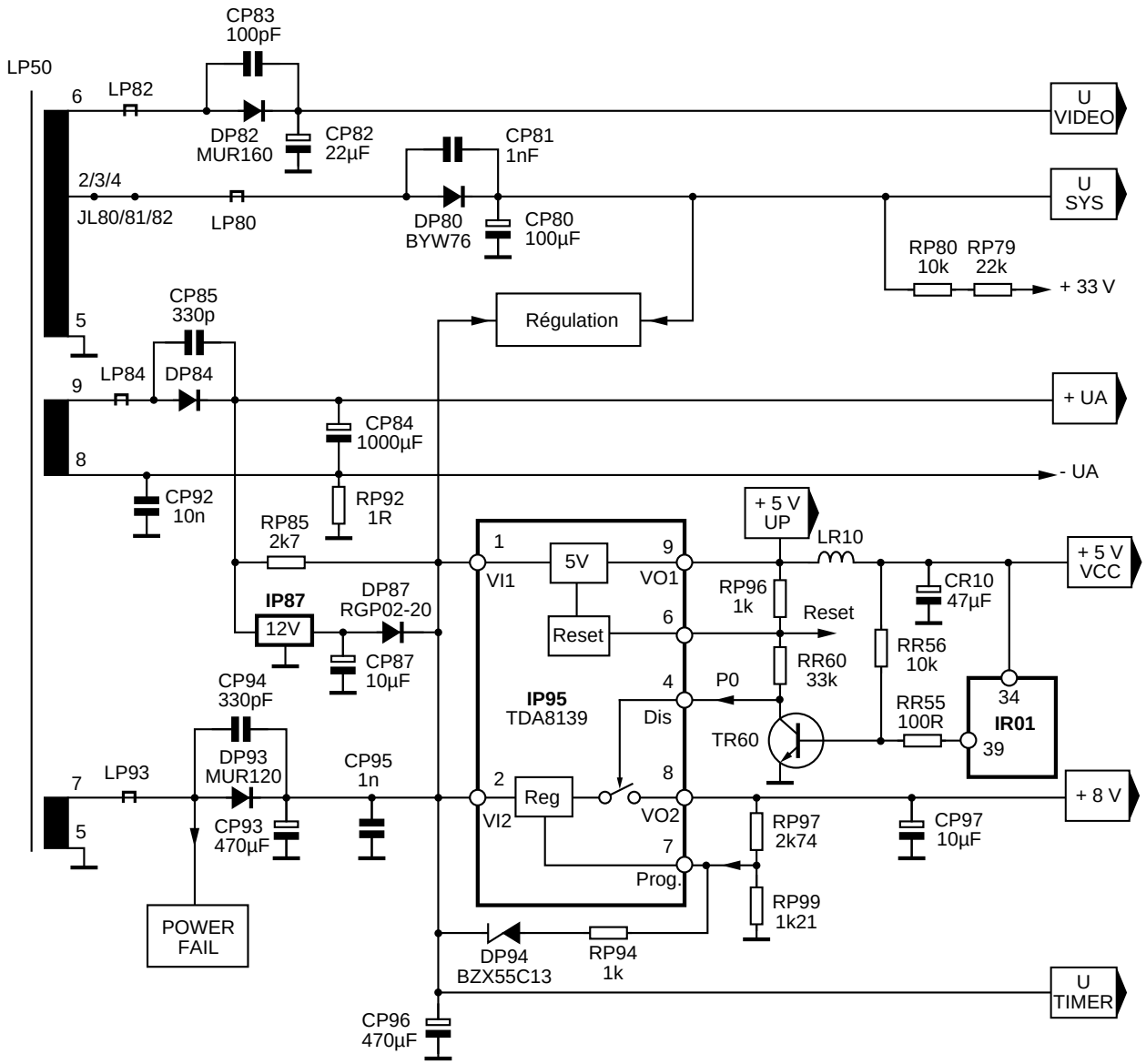
SECONDARY REGULATION

SECONDARY REGULATION

Secondary regulation operates:
- in TIMER mode where it stabilises the secondary voltages at 50% of the rated value (to limit the power consumed).
- in ON mode when it regulates the USYS voltage to its rated value
- in an intermediary mode during the changeover from TIMER mode to ON mode when the secondary voltages are stabilised at 75% of their rated value.

In TIMER mode TP76 conducts and controls TP75. The voltage obtained on the ref-pin of IP61 via DP70 and RP62 fixes the secondary voltages at 50% of their value (first threshold).
During start-up, TP82 takes over from TP75 which is now blocked to stabilise the secondary voltages at 75% of their value (second threshold).
Finally, TP82 is again blocked, as is TP70 and it is a fraction of USYS (via RL65 and RP63) which controls IP61 (adjustable by PP64) to stabilise the voltage at its rated value.

Note that in TIMER mode, the regulation works in salvo mode.



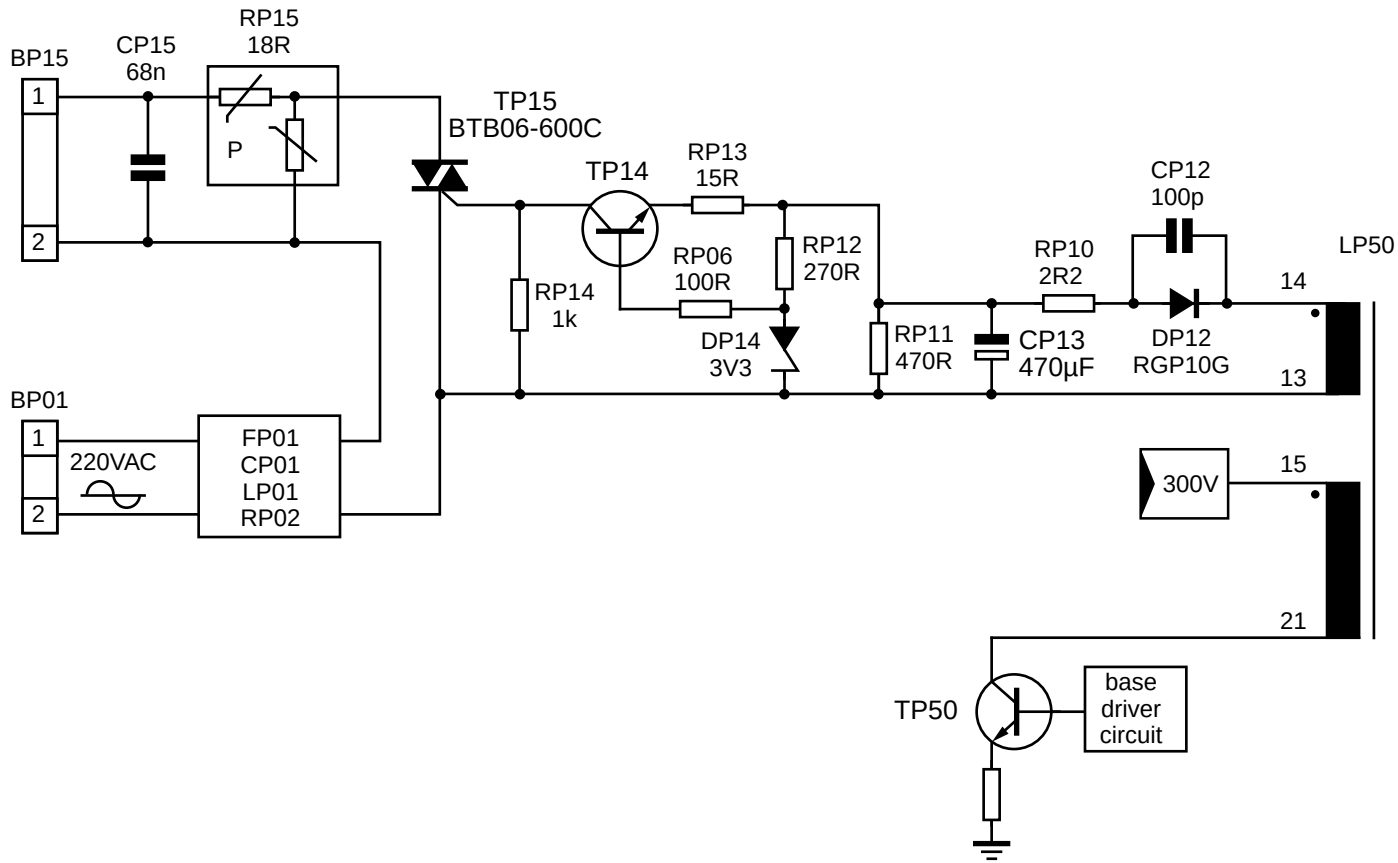
SECONDARIES DISTRIBUTION

SECONDARIES

It should be recalled that the 4 secondary windings supply respectively:
- the Uvideo voltage of 200 volts +/- 8 volts (rated I = 10 mA)
- USYS of 126 to 138 volts depending on the tube (max I = 700 mA)
- + UA of 29 volts (maximum load) to 35 volts (minimum load) (max I = 1.2 A)
- UTIMER of 12 volts +/– 1 volt (rated I = 100 mA)

The circuit IP95 supplies:
- the permanent 5 VUP and reset for management
- 8 volts for supplying the video processor switched by the micro controller via the PO command.

Power supply to IP95 is provided during normal regimen by the UTIMER voltage (12 V).
However, in TIMER mode, since this voltage is lower, it is the + UA which takes over via IP87 and DP87.

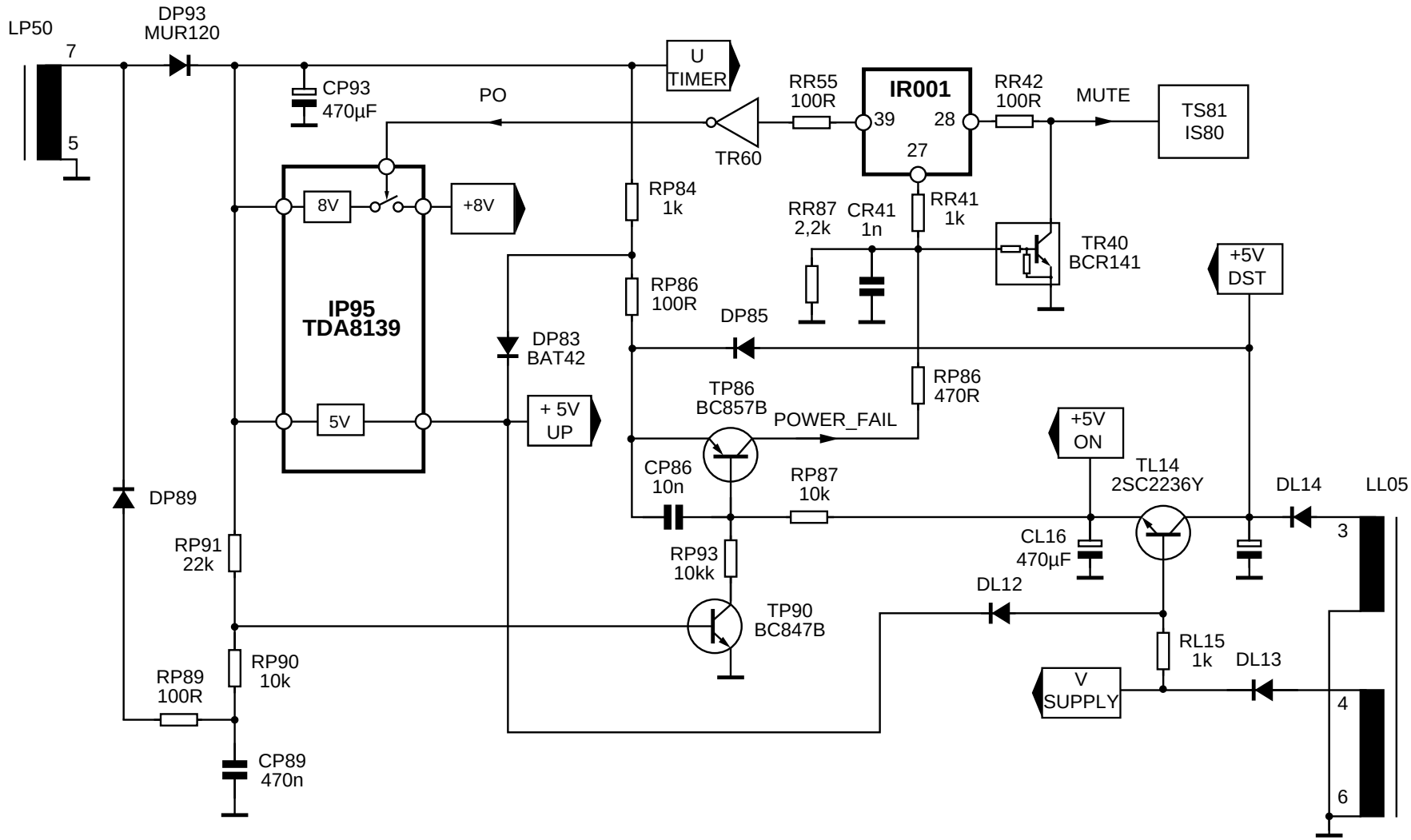


TUBE DEMAGNETISATION

36

TUBE DEMAGNETISATION CIRCUIT

In stand-by, no voltage appears at capacitor CP13. Transistor TP14 is blocked, as well as the triac TP15.
In TIMER mode, the charge of CP13 is –1V5, a voltage which is inadequate to polarise the zener DP14 (3V3), TP14 remains blocked.
During start-up in normal regimen, the second regulation threshold (see corresponding chapter) limits voltages to 75% of their value, the CP13 is charged to –2V5.
The triac is still blocked.
Finally, since scanning has started, the capacitor CP13 changes to –5V, TP14 and TP15 conduct, the posistor is supplied and a decreasing current from the mains crosses the demagnetisation loop.



CIRCUIT POWER-FAIL

MAINS POWER CUT DETECTION CIRCUIT

If mains power falls below 150 V AC, the voltage at the terminals of CP89 increases above –4.4 volts and TP90 is polarised. Transistors TP90 and TP86 conduct, the Power Fail line changes to high status and informs the micro controller which cuts off the 8 volts switched by the PO line.
This assembly also controls the THT through DP85, DP86 and TP86 under the following conditions:

- in the case of over voltage of the THT secondaries, the increase in the +5 VDST results in conduction at TP86. The micro controller then stops scanning before attempting a restart 2 seconds later. If this is unsuccessful after the third attempt, the micro controller forces stand-by mode.
- in the case of under voltage of the +5 V ON, the transistor TP86 is freed and enables the Power Fail information with the same effect as above.

Note that the micro controller uses this means to control start-up of THT.

TIME BASE

CONTENTS

INTRODUCTION

GENERATION OF THE TDA 8855H COMMAND SIGNALS

DRIVER STAGE

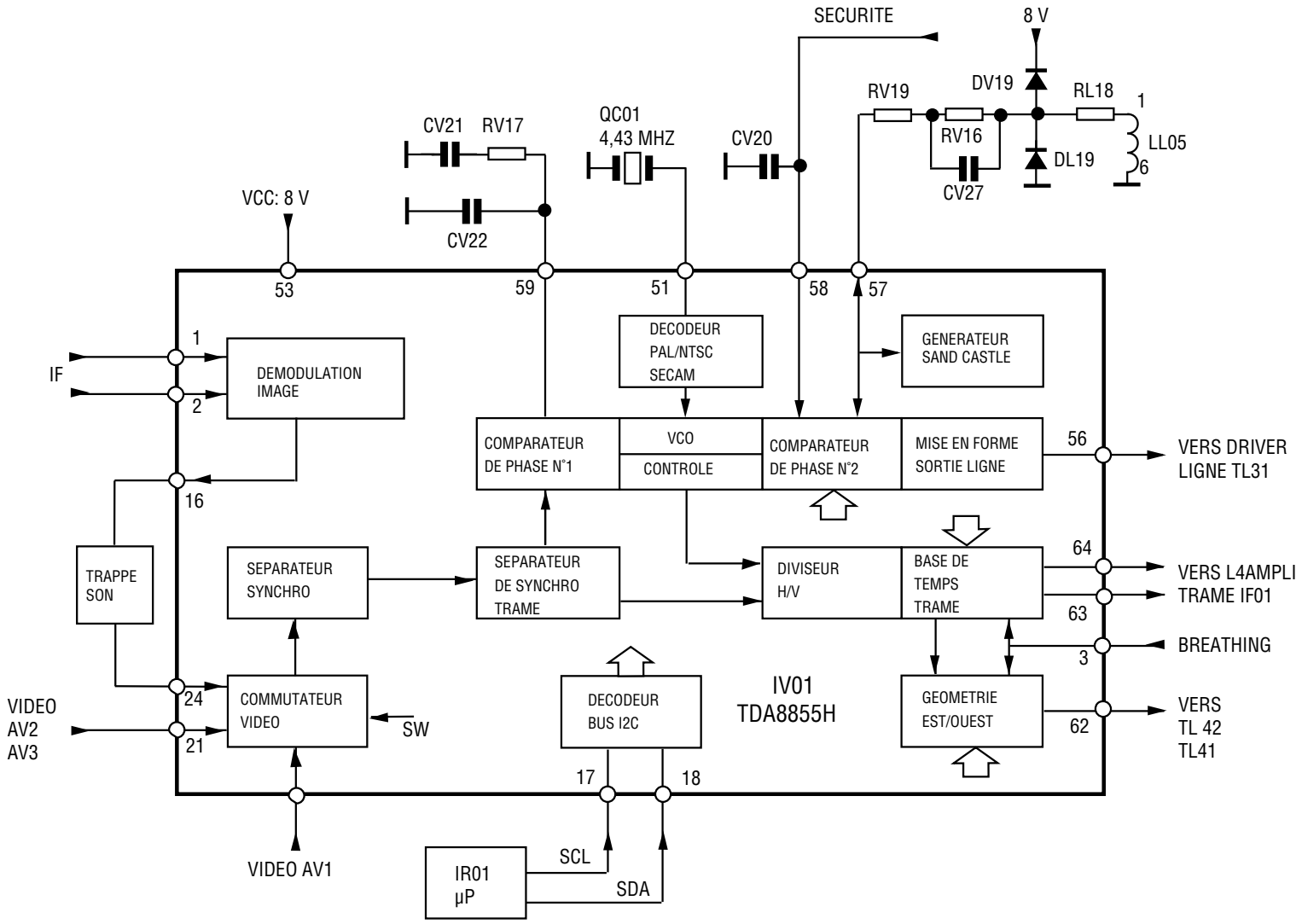
LINE POWER AND THT

EW STAGE

FORMAT CORRECTION

FRAME SCANNING

TIME BASE SAFETY

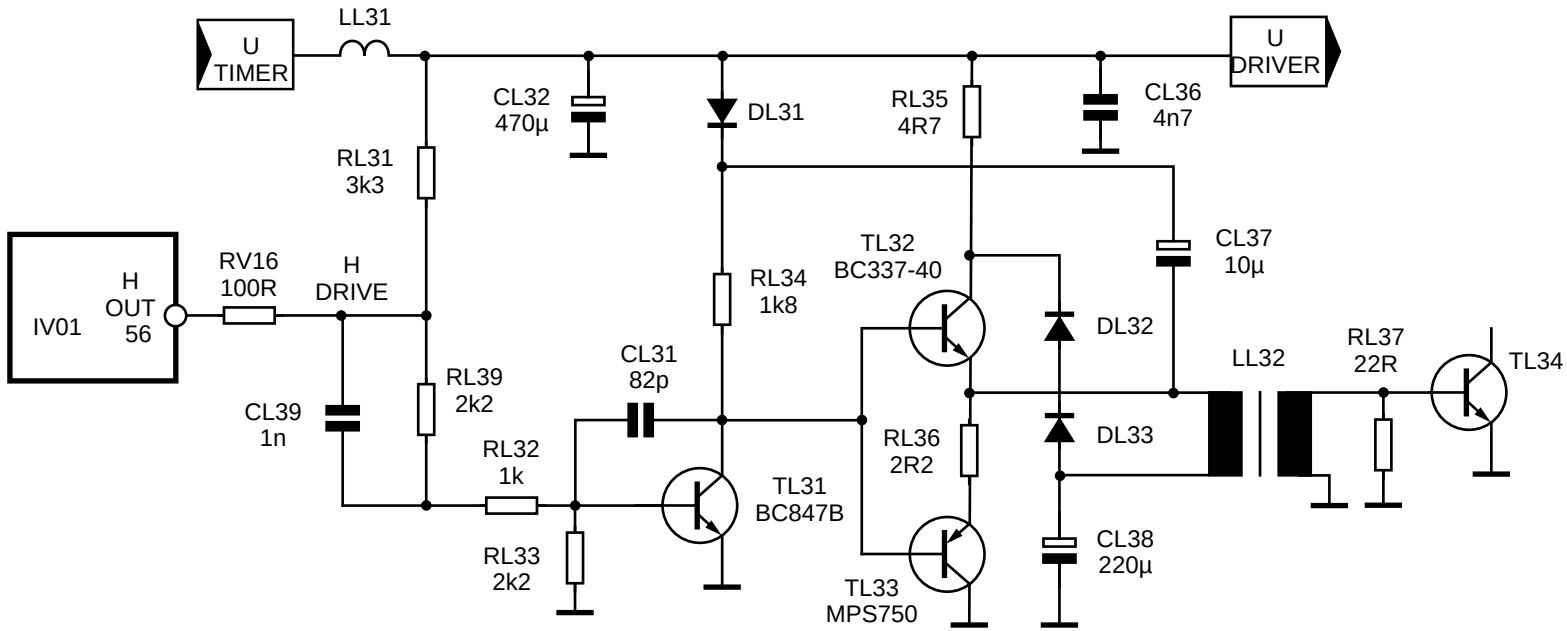

SECURITE
8 V
RV19
DV19
RL18
1
LL05
6
RV16
DL19
CV27
CV21
RV17
CV22
QC01
4,43 MHZ
CV20
VCC: 8 V
53
59
51
58
57
DECODEUR
PAL/NTSC
SECAM
GENERATEUR
SAND CASTLE
IF
1
2
DEMODULATION
IMAGE
COMPARATEUR
DE PHASE N°1
VCO
CONTROLE
COMPARATEUR
DE PHASE N°2
MISE EN FORME
SORTIE LIGNE
56
VERS DRIVER
LIGNE TL31
16
TRAPPE
SON
SEPARATEUR
SYNCHRO
SEPARATEUR
DE SYNCHRO
TRAME
DIVISEUR
H/V
BASE DE
TEMPS
TRAME
64
VERS L4AMPLI
TRAME IF01
63
BREATHING
3
VIDEO
AV2
AV3
24
21
COMMUTATEUR
VIDEO
SW
DECODEUR
BUS I2C
IV01
TDA8855H
GEOMETRIE
EST/OUEST
62
VERS
TL 42
TL41
17
18
VIDEO AV1
IR01
µP
SCL
SDA

INTRODUCTION

Time base commands are generated by the video processor IV01: TDA 8855H
The latter is supplied with power from the 8 V voltage at pin 53.
This voltage is available in "ON" mode.
The 12C BUS is present on pins 17 and 18.

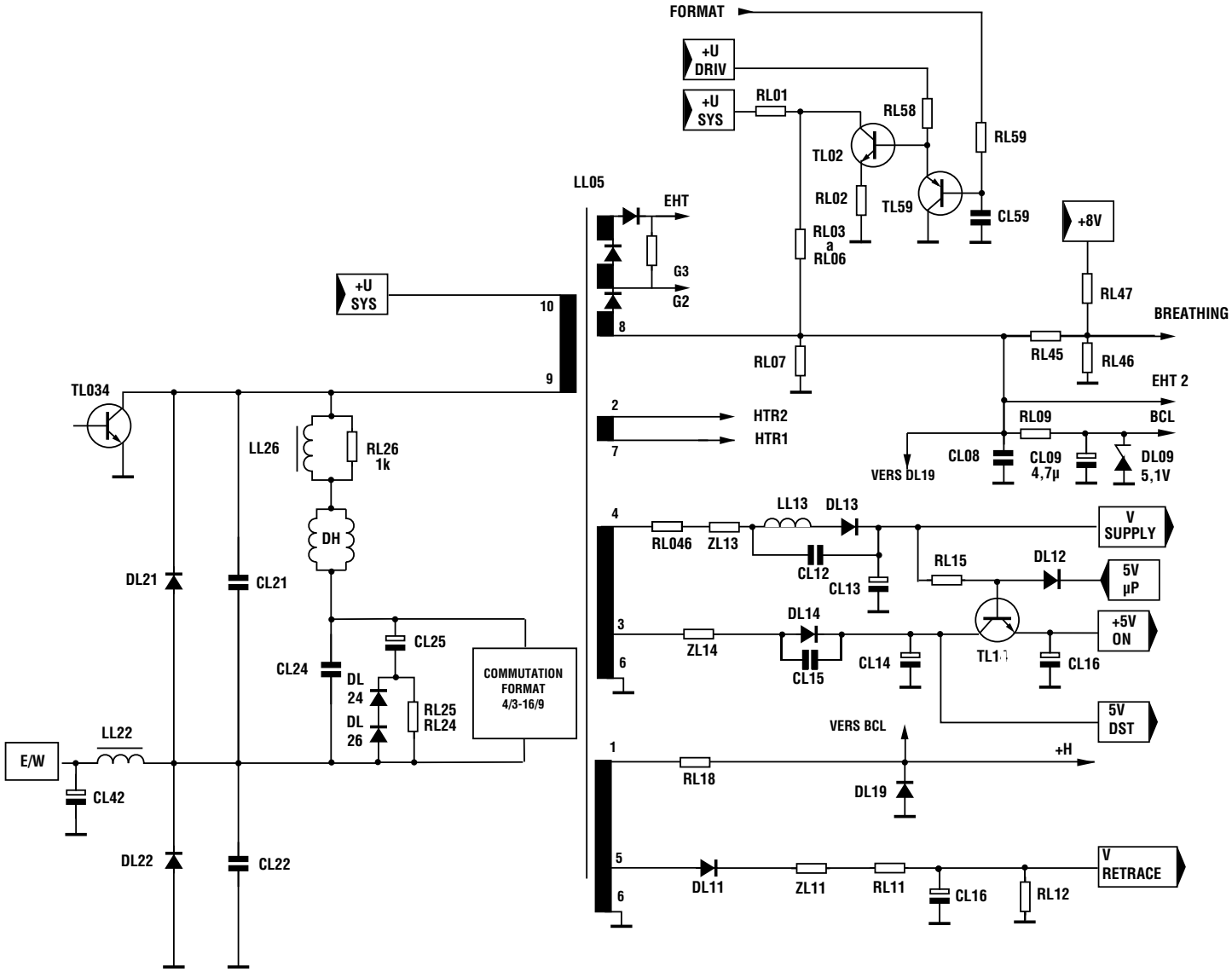
GENERATION OF THE LINE COMMAND

A VCO and divider assembly managed by the 4.43 MHZ quartz (pin 51) supplies a signal at line frequency.
A first phase comparator, on receiving the video signal line synchronisation, locks the divider.
A second phase comparator ensures static phasing. It receives line return pulses from pin 1 of transformer THT LL05 on pin 57.
The line signal, after a formatting stage, is present at pin 56 of IV01 and is then sent to the line power transistor TL54 via the driver stage.


U
TIMER
LL31
U
DRIVER
CL32
470µ
DL31
RL35
4R7
CL36
4n7
RL31
3k3
CL37
10µ
TL32
BC337-40
IV01
H
OUT
56
RV16
100R
H
DRIVE
RL34
1k8
DL32
LL32
RL37
22R
TL34
CL31
82p
RL39
2k2
CL39
1n
RL36
2R2
DL33
RL32
1k
TL31
BC847B
RL33
2k2
CL38
220µ
TL33
MPS750

DRIVER STAGE

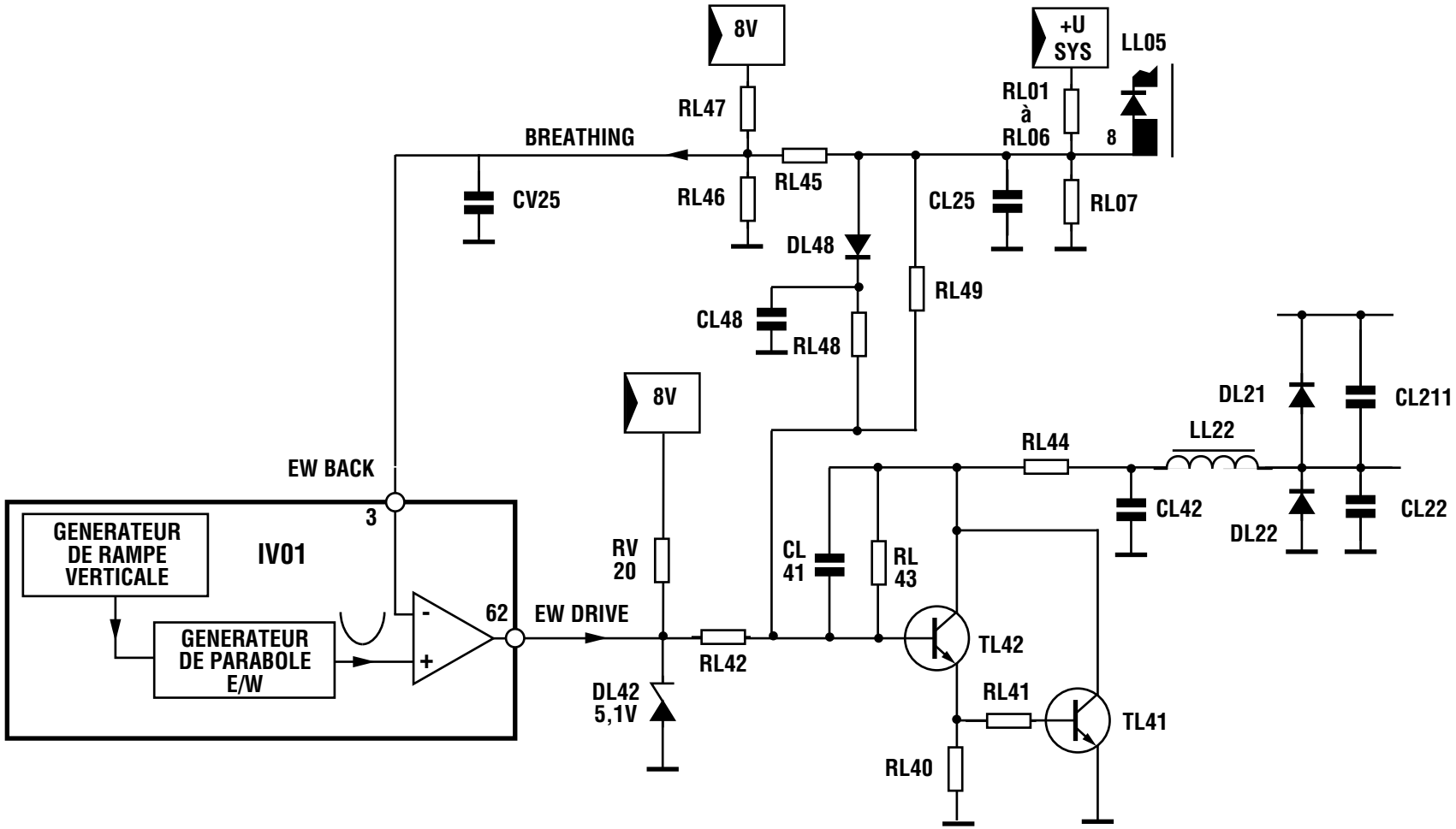
The line transistor is controlled by the intermediary of a driver transformer operating in forward mode. Its primary is permanently crossed by a positive or negative current.
For this purpose, the base of the primary LL32 relies on positive voltage from the charge of capacitor CL38 linked to the cyclical ratio of the line command. The transistor driver TL 31 switched by this signal controls the push-pull TL 32/TL 33.
Diodes DL32/DL 33 intervene in the case of a short-circuit between the collector/transmitter of transistor TL 32 to render the TV set safe by stopping scanning. From this time TL 33 conducts permanently and causes rapid destruction of RL35.


FORMAT
+U DRIV
+U SYS
RL01
RL58
RL59
TL02
RL02
TL59
CL59
RL03 a RL06
+8V
LL05
EHT
G3
G2
+U SYS
10
9
8
RL07
RL47
BREATHING
RL45
RL46
EHT 2
TL034
LL26
RL26 1k
2
7
HTR2
HTR1
RL09
BCL
CL08
CL09 4,7µ
DL09 5,1V
VERS DL19
DH
4
LL13
DL13
V SUPPLY
RL046
ZL13
CL12
CL13
RL15
DL12
5V µP
DL21
CL21
3
DL14
+5V ON
ZL14
CL14
CL15
CL16
CL24
CL25
DL 24
DL 26
RL25 RL24
COMMUTATION FORMAT 4/3-16/9
6
5V DST
VERS BCL
LL22
E/W
1
+H
RL18
DL19
CL42
DL22
CL22
5
DL11
ZL11
RL11
CL16
RL12
V RETRACE
6

LINE POWER AND THT

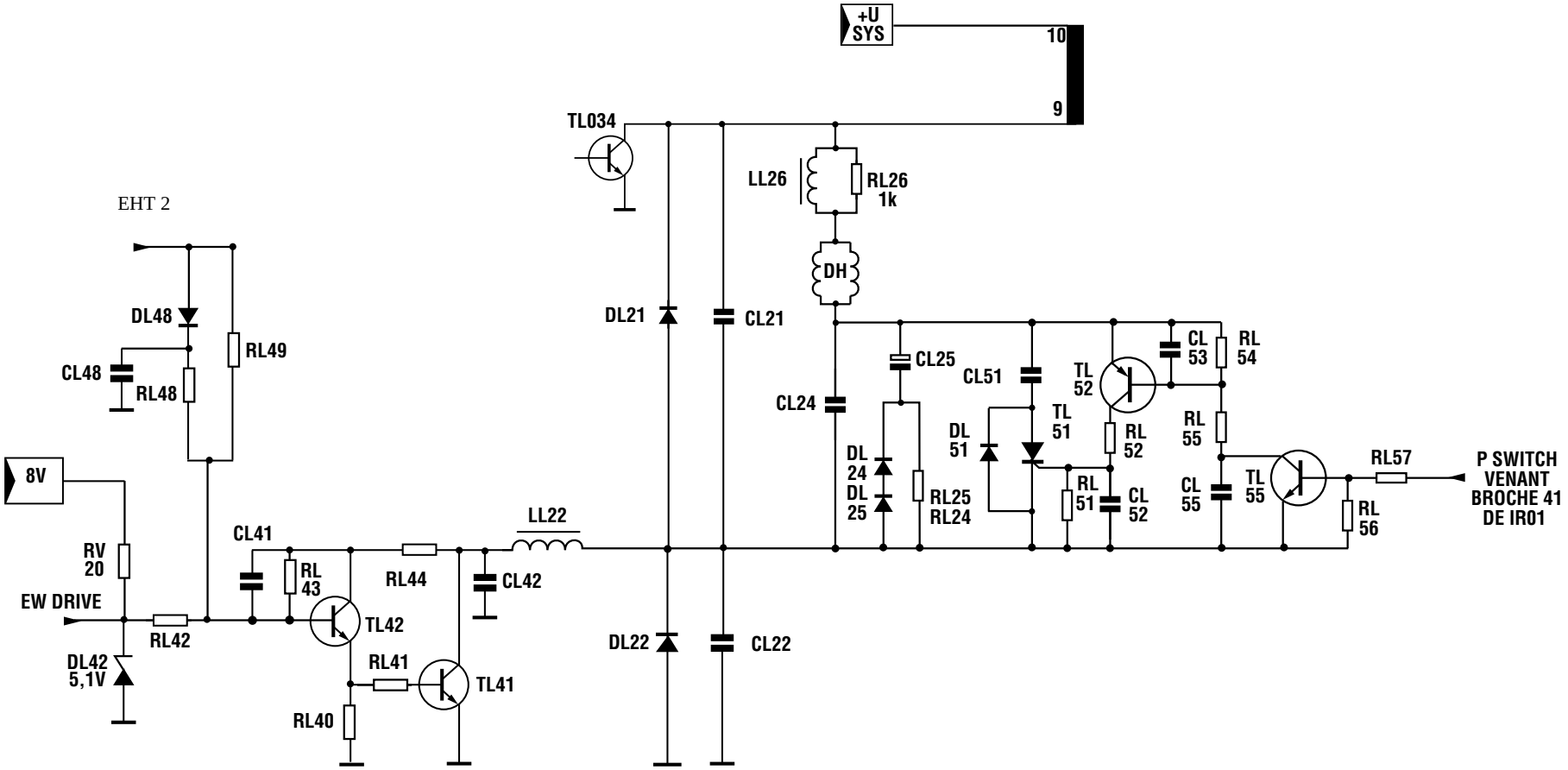
The LL05 primary supplied by the + USYS voltage is associated with the line power transistor TL34 and the diode modulator DL21, DL22, CL21, CL22.
These switching components also channel current from the horizontal deviator connected in serial with the capacitor of "S " CL24 and the linearity inductance coil LL26.
Two circuits are assembled in parallel on the capacitor "S". The first is a damping circuit to suppress oscillations which appear during rapid changes in beam current. The second on the 16/9 rack only, allows by adding a capacitor switched by a thyristor, adjusting line amplitude during changes of format.

On the LL05 secondaries the following are located:
- pin 2 and 7 a pulse for heating the image tube filament.
- pin 4 rectified by DL13 filtered by CL13 "V SUPPLY" voltage.
- pin 3 rectified by DL14 filtered by CL14 and stabilised by TL14 from the 5 Vmp with a voltage of 5V ON.
- pin 1 a positive line return pulse to obtain service signals.
- pin 5 rectified by DL11 filtered by CL16 a "V RETRACE" voltage to supply the frame amplifier during return.
- pin 8 the image of the instantaneous beam current "BREATHING", "bcl", "EHT 2".


8V
+U SYS
LL05
RL01 à RL06
8
RL47
BREATHING
RL46
RL45
CV25
CL25
RL07
DL48
RL49
CL48
RL48
8V
DL21
CL211
LL22
RL44
EW BACK
3
GENERATEUR DE RAMPE VERTICALE
IV01
CL42
DL22
CL22
RV 20
CL 41
RL 43
GENERATEUR DE PARABOLE E/W
-
+
62
EW DRIVE
TL42
RL42
DL42 5,1V
RL41
TL41
RL40

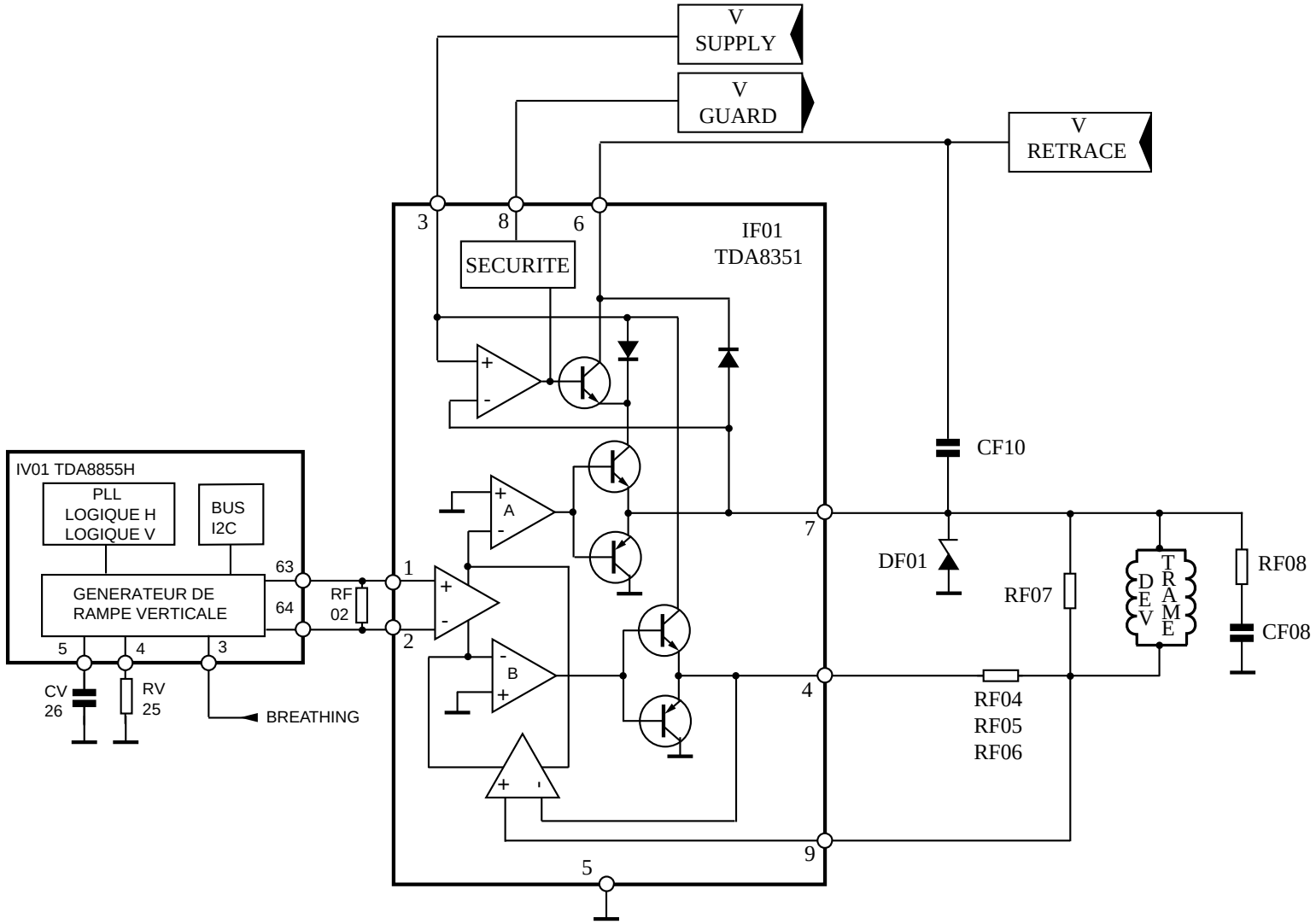
EW STAGE

The integrated circuit IV01 integrates the E/W parabola generator synchronised by the vertical ramp generator.
The various adjustments are by the intermediary of service mode and are routed by the 12C bus.
An amplifier integrated in IV01 supplies in the form of a parabolic current at pin 62 an E/W command, which is applied at two transistors TL 41 and TL 42 assembled in darlington. It extract energy from the modulator through the inductance coil LL22.
From the EHT2 voltage image of the beam current and through DL48, RL48, RL49, CL48, automatic correction of width is made depending on the tube rate.


EHT 2
+U SYS
10
9
TL034
LL26
RL26 1k
DH
DL48
RL49
CL48
RL48
DL21
CL21
CL25
CL51
TL 52
CL 53
RL 54
CL24
TL 51
RL 55
DL 51
RL 52
DL 24
DL 25
RL25 RL24
RL 51
CL 52
CL 55
TL 55
RL57
RL 56
P SWITCH VENANT BROCHE 41 DE IR01
8V
LL22
CL41
RV 20
RL 43
RL44
CL42
EW DRIVE
TL42
RL42
DL22
CL22
DL42 5,1V
RL41
TL41
RL40

FORMAT CORRECTION

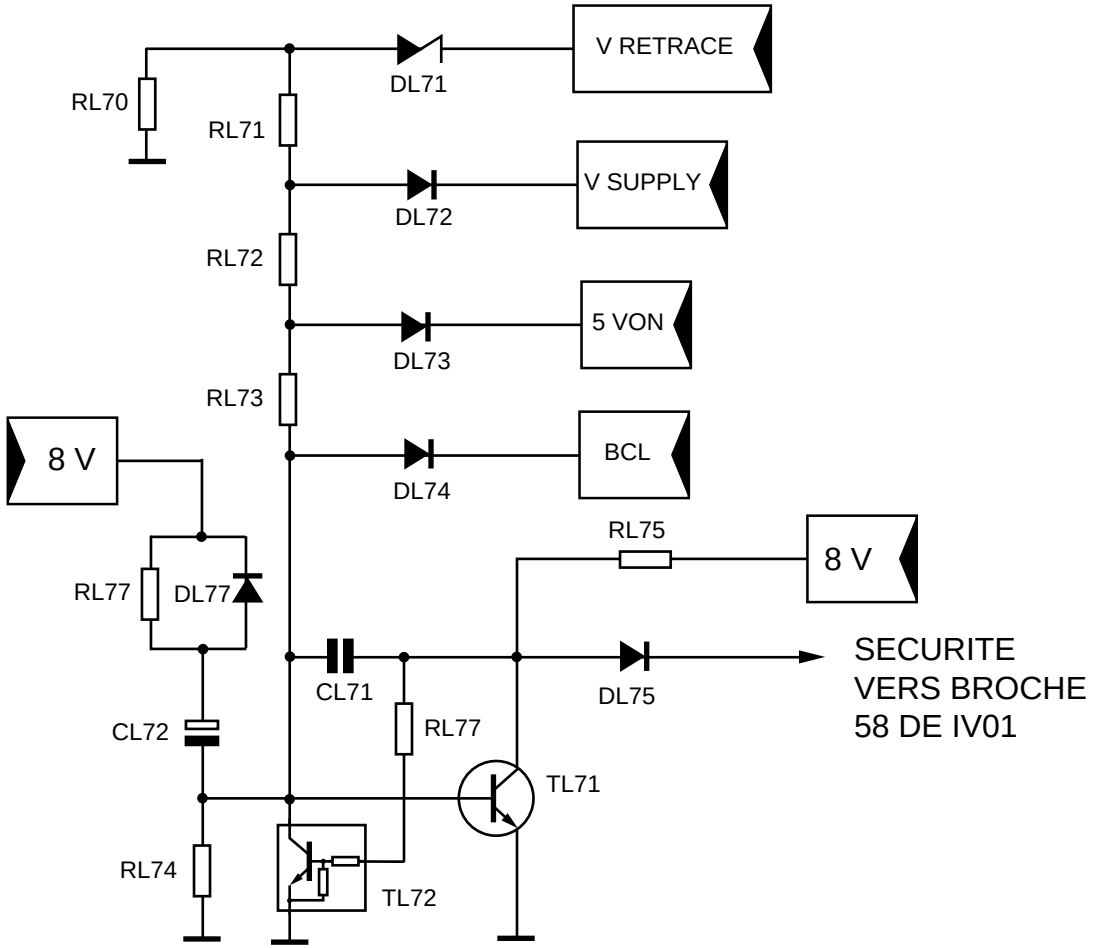
On the 16/9 rack it is possible to switch via the intermediary of TL55, TL52, TL51 controlled by the IR01 µp, a second capacitor "S" CL51 in parallel on CL24.
The effect is to reduce line amplitude and supply correct linearity in centred 4/3 mode.


V
SUPPLY
V
GUARD
V
RETRACE
IF01
TDA8351
SECURITE
3
8
6
7
4
9
5
1
2
CF10
DF01
RF07
RF08
CF08
TRAME DEV
RF04
RF05
RF06
IV01 TDA8855H
PLL
LOGIQUE H
LOGIQUE V
BUS
I2C
GENERATEUR DE
RAMPE VERTICALE
63
64
RF
02
5
4
3
CV
26
RV
25
BREATHING
A
B

FRAME SCANNING

Two circuits are involved in frame scanning.
IV01 (TDA8855H) generates the frame saw tooth
IF01 (TDA8351) amplifies this signal and supplies the signal to the frame deviator

The video processor IV01 incorporates a vertical ramp generator which uses the capacitor CV26 (pin 5) and the resistor RV25 (pin 4).
The amplitude of this ramp is adjusted versus the BREATHING information applied at pin 3 (automatic height correction).
Linearity and amplitude correction is also supplied by IV01. They can be adjusted by bus 12C in the framework of service mode. A correct border is ensured by internal continuous voltage adjusted at bus 12C.
A saw tooth signal is available at pin 64 combined with a continuous component on pin 63 to control the amplifier circuit IF01.
The circuit TDA 8351 receives the previous commands at pins 1 and 2.
The voltages V SUPPLY and V RETRACE supply this circuit.
The output pin 5 supplies current to the deviator. In series with the latter, the resistors RF04, RF05, RF06 develop at their terminals, an image of the current for the counter reaction.
To avoid burning the image tube in the event of frame failure, we monitor satisfactory operation of the frame time base by the GUARD data which will be at high status. In the case of a frame failure, absence of this data indicates to the video processor IV01 (pin 34) a defect, and the latter cuts the three RGB channels by rendering the circuit safe after two start-up attempts (failure code 27).


V RETRACE
DL71
RL70
RL71
V SUPPLY
DL72
RL72
5 VON
DL73
RL73
8 V
BCL
DL74
RL75
8 V
RL77
DL77
CL71
DL75
SECURITE
VERS BROCHE
58 DE IV01
CL72
RL77
TL71
RL74
TL72

TIME BASE SAFETY

The safety circuit detects short circuits in scanning or line voltages and runaway of the beam current.
The frame deviator signal supplies a voltage which polarises the zener DL71 and saturates the transistor TL71 imposing a low level on the SAFETY line.
The following defects force a high level on the SAFETY line, which applied at pin 58 of IV01 cuts off line scanning.

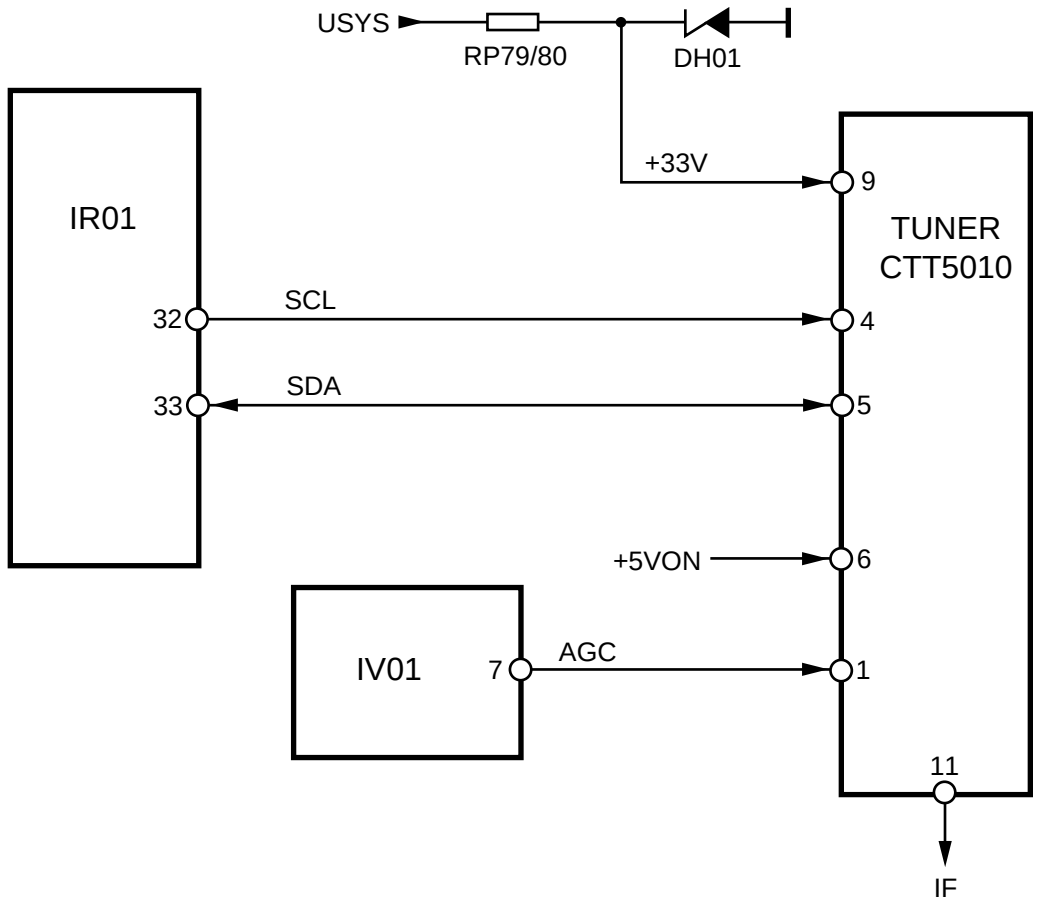
- Frame defect by DL71.
- Defect in the V SUPPLY voltage by DL72.
- Defect in the 5V On voltage by DL73.
- Runaway of the beam current.

HIGH FREQUENCY
INTERMEDIATE FREQUENCY

CONTENTS

CTT5010 TUNER

INTERMEDIATE FREQUENCIES

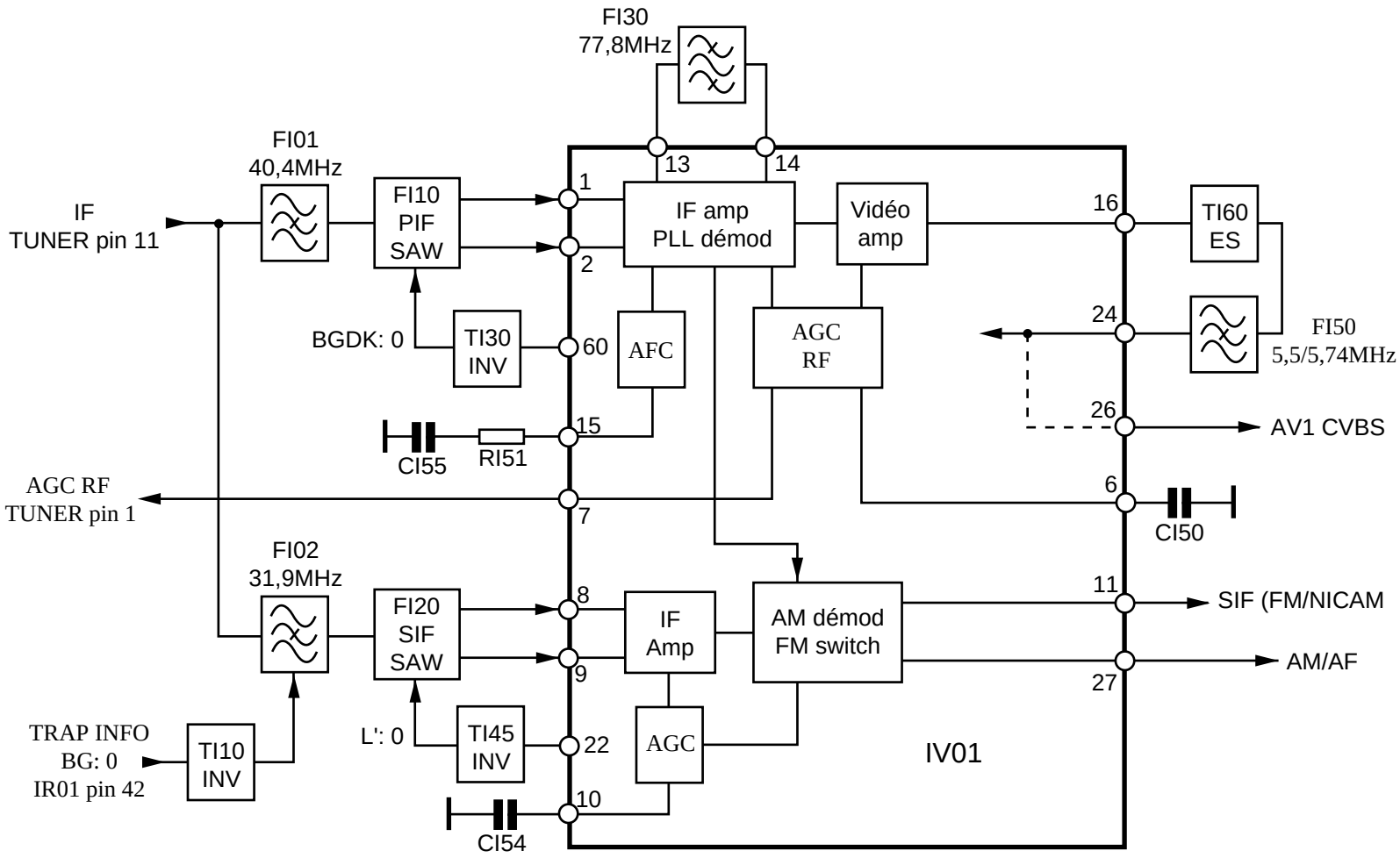

USYS
RP79/80
DH01
+33V
9
IR01
TUNER
CTT5010
SCL
32
4
SDA
33
5
+5VON
6
IV01
7
AGC
1
11
IF

58

CTT5010 TUNER

The CTT5010 is a tuner equipped with frequency synthesis. It is controlled by the µC IR01 via the IIC bus for switching standards and channel management. It covers the following frequency ranges :

- VL : 48.25 MHz to 112.25 MHz
- VH : 119.25 MHz to 399.25 MHz
- U : 407.25 MHz to 863.25 MHz


FI30
77,8MHz
FI01
40,4MHz
IF
TUNER pin 11
FI10
PIF
SAW
1
2
13
14
IF amp
PLL démod
Vidéo
amp
16
TI60
ES
BGDK: 0
TI30
INV
60
AFC
AGC
RF
24
FI50
5,5/5,74MHz
26
AV1 CVBS
CI55
RI51
15
AGC RF
TUNER pin 1
7
6
CI50
FI02
31,9MHz
FI20
SIF
SAW
8
9
IF
Amp
AM démod
FM switch
11
SIF (FM/NICAM
AM/AF
27
TRAP INFO
BG: 0
IR01 pin 42
TI10
INV
L': 0
TI45
INV
22
AGC
IV01
10
CI54

INTERMEDIATE FREQUENCIES

IMAGE INTERMEDIATE FREQUENCY

The IF from output 11 of the tuner passes through filter IF01 (rejection of adjacent channel in BG, 40.4 MHz), the IF10 grouped selectivity and is then fed to IV01 by its pins 1 and 2.
Filter IF10 can be switched. For LL'IK' standards it has two nyquist sides (38.9 MHz and 33.9 MHz). For BGDK standards it has 1 nyquist side (38.9 MHz).
In IV01 the image IF is amplified and demodulated. The video signal, supplied at 16 of IV01 passes through the FM audio inter-carriers rejector (IF50) and fed back at 24 of IV01. In IV01 it is sent to the switching stage and output 26 for the SCART socket AV1.
The CAG HF voltage present at output 7 of IV01 (0.5V to 4.1V) is transmitted to the tuner.

SOUND INTERMEDIATE FREQUENCY

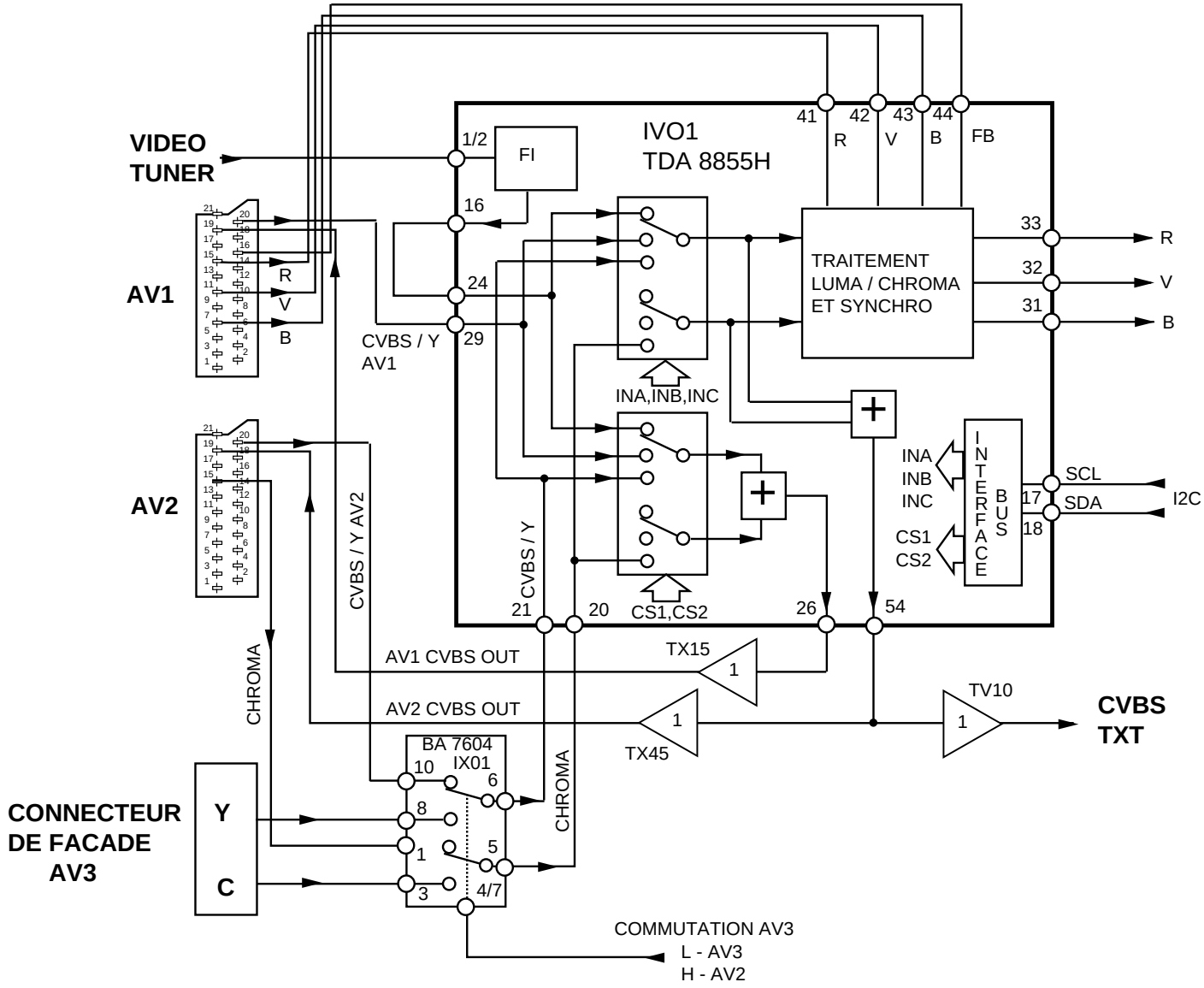
The IF from output 11 of the tuner passes through filter IF02 (rejection of adjacent channel in BG, 31.9 MHz), the IF20 grouped selectivity and is then fed to IV01 by its pins 8 and 9.
Filter IF20 can be switched. For L' standards, its accord frequency is 40.4 MHz. For other standards, its accord frequency is 32.4 MHz.
In IV01, the AM sound IF is amplified, demodulated and supplied at output 27.
In IV01, the FM sound IF and the NICAM, sampled from the video stages are amplified and supplied at output 11.

SWITCHING

CONTENTS

VIDEO SWITCHING

RGB SWITCHING


VIDEO
TUNER
AV1
AV2
R
V
B
1/2
FI
IVO1
TDA 8855H
16
24
29
CVBS / Y
AV1
41
42
43
44
R
V
B
FB
TRAITEMENT
LUMA / CHROMA
ET SYNCHRO
33
32
31
R
V
B
INA,INB,INC
CS1,CS2
INA
INB
INC
CS1
CS2
INTERFACE BUS
17
18
SCL
SDA
I2C
CVBS / Y AV2
CVBS / Y
21
20
26
54
CHROMA
AV1 CVBS OUT
AV2 CVBS OUT
TX15
TX45
TV10
1
CVBS
TXT
BA 7604
IX01
10
6
8
1
5
3
4/7
CHROMA
CONNECTEUR
DE FACADE
AV3
Y
C
COMMUTATION AV3
L - AV3
H - AV2

VIDEO SWITCHING

The integrated circuit IV01 allows switching the 7 input sources (VIDEO or Y/C) to 2 outputs for the SCART sockets and the teletext and 1 internal output for the processing channel. The µC IR01 controls switching via the I2C bus.
The voltages from pin 8 of the SCART sockets arriving at pins 36 and 37 of µC IR01 indicate, depending on their values, a 4/3 or 16/9 source.
Switching between the SCART socket AV2 and AV3 is by the data "AV3 PORT" from pin 40 of µC IR01.

RGB SWITCHING

The RGBs for the SCART socket AV1 are present at pins 41, 42, 43 of the integrated circuit IV01. The rapid switching signal present at pin 44 switches between signals from the video source switch and the RGBs.

VIDEO PROCESSING

CONTENTS

GENERAL

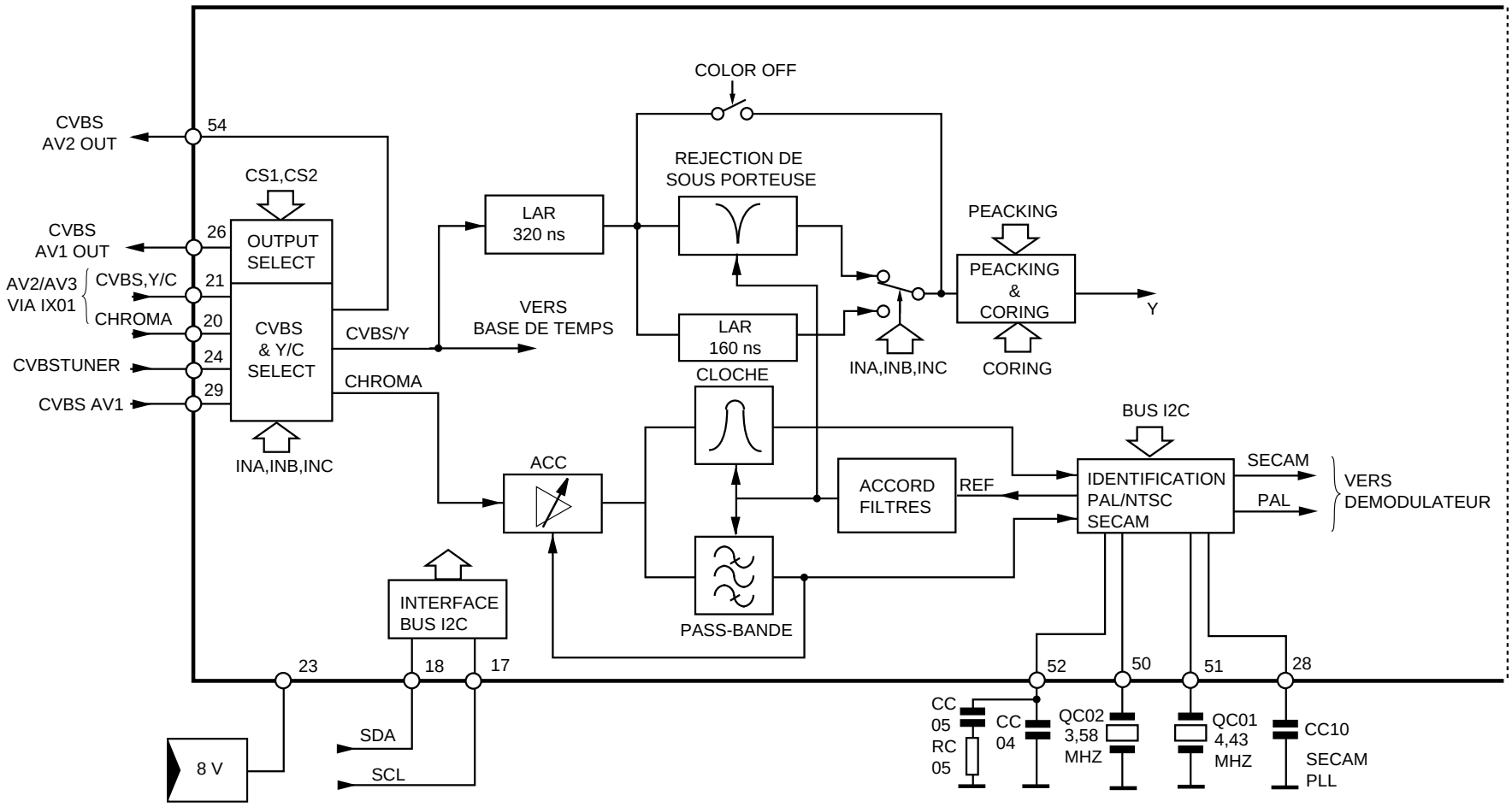
LUMINANCE/CHROMINANCE SEPARATION

CHROMA IDENTIFICATION

CHROMA DEMODULATION

SWITCHING OF RGB AV1 AND OSD

PROCESSING RGB


COLOR OFF
CVBS
AV2 OUT
54
CS1,CS2
REJECTION DE
SOUS PORTEUSE
LAR
320 ns
PEACKING
CVBS
AV1 OUT
26
OUTPUT
SELECT
AV2/AV3
VIA IX01
CVBS,Y/C
21
CHROMA
20
VERS
BASE DE TEMPS
LAR
160 ns
PEACKING
&
CORING
Y
CVBS
& Y/C
SELECT
CVBS/Y
CVBSTUNER
24
CLOCHE
INA,INB,INC
CORING
CVBS AV1
29
CHROMA
BUS I2C
ACC
ACCORD
FILTRES
REF
IDENTIFICATION
PAL/NTSC
SECAM
SECAM
PAL
VERS
DEMODULATEUR
INTERFACE
BUS I2C
PASS-BANDE
23
18
17
52
50
51
28
8 V
SDA
SCL
CC
05
RC
05
CC
04
QC02
3,58
MHZ
QC01
4,43
MHZ
CC10
SECAM
PLL

GENERAL

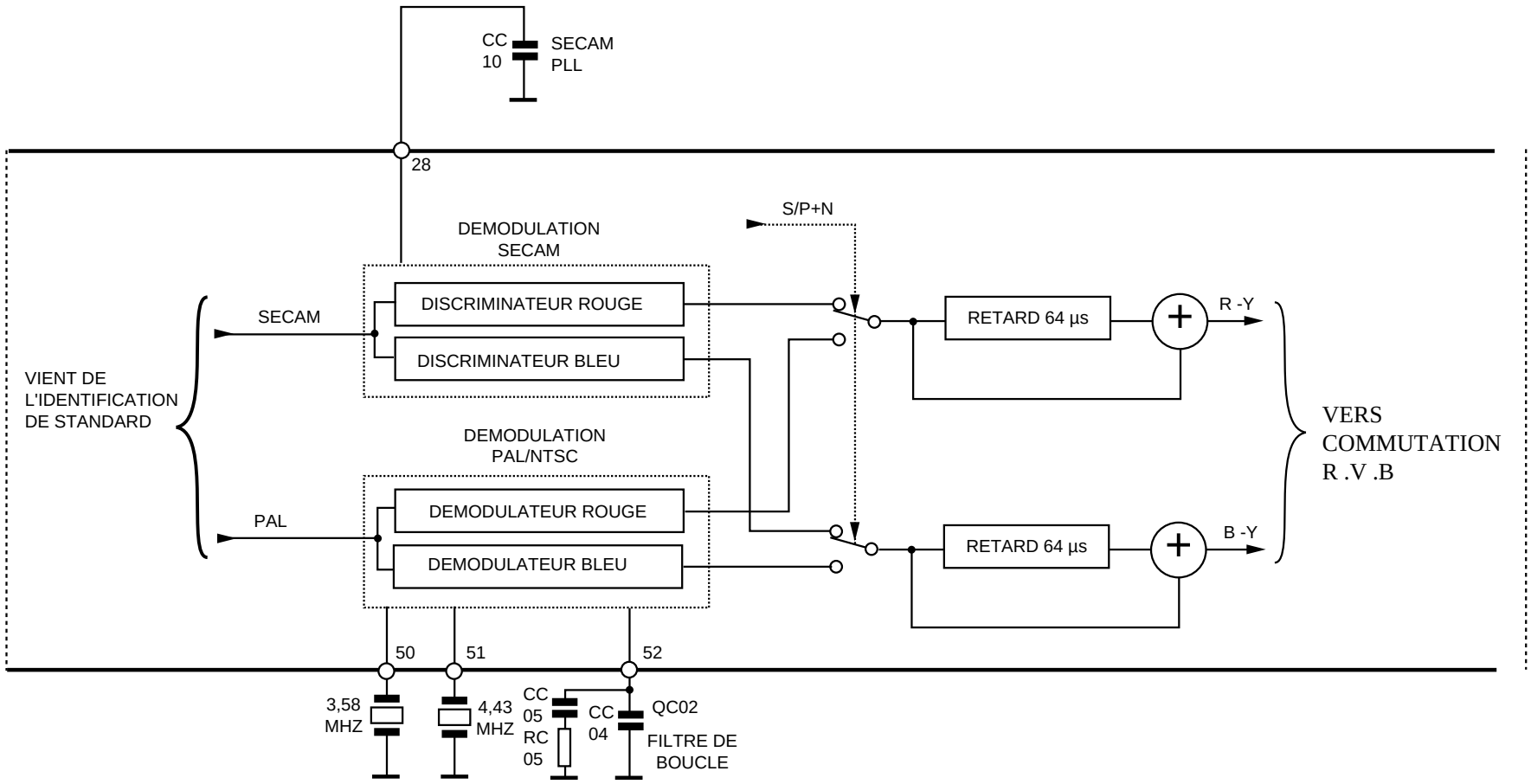
All luminance and chrominance processing is performed inside integrated circuit IV01 TDA 8855H. Integration was increased and very few components are external to the integrated circuit.
The power supply of this circuit with 8 V is located on pin 23, the I2C bus allowing control of video processing.

LUMINANCE/CHROMINANCE SEPARATION

The composite video signal switched for processing is applied to the sub carrier rejection stage accorded automatically with the standard detected.
In Y/C mode the sub carrier rejector is suppressed.
The luminance signal passes through the contour adjustment circuit and a noise reducer prior to being switched with the signals R-Y and B-Y.

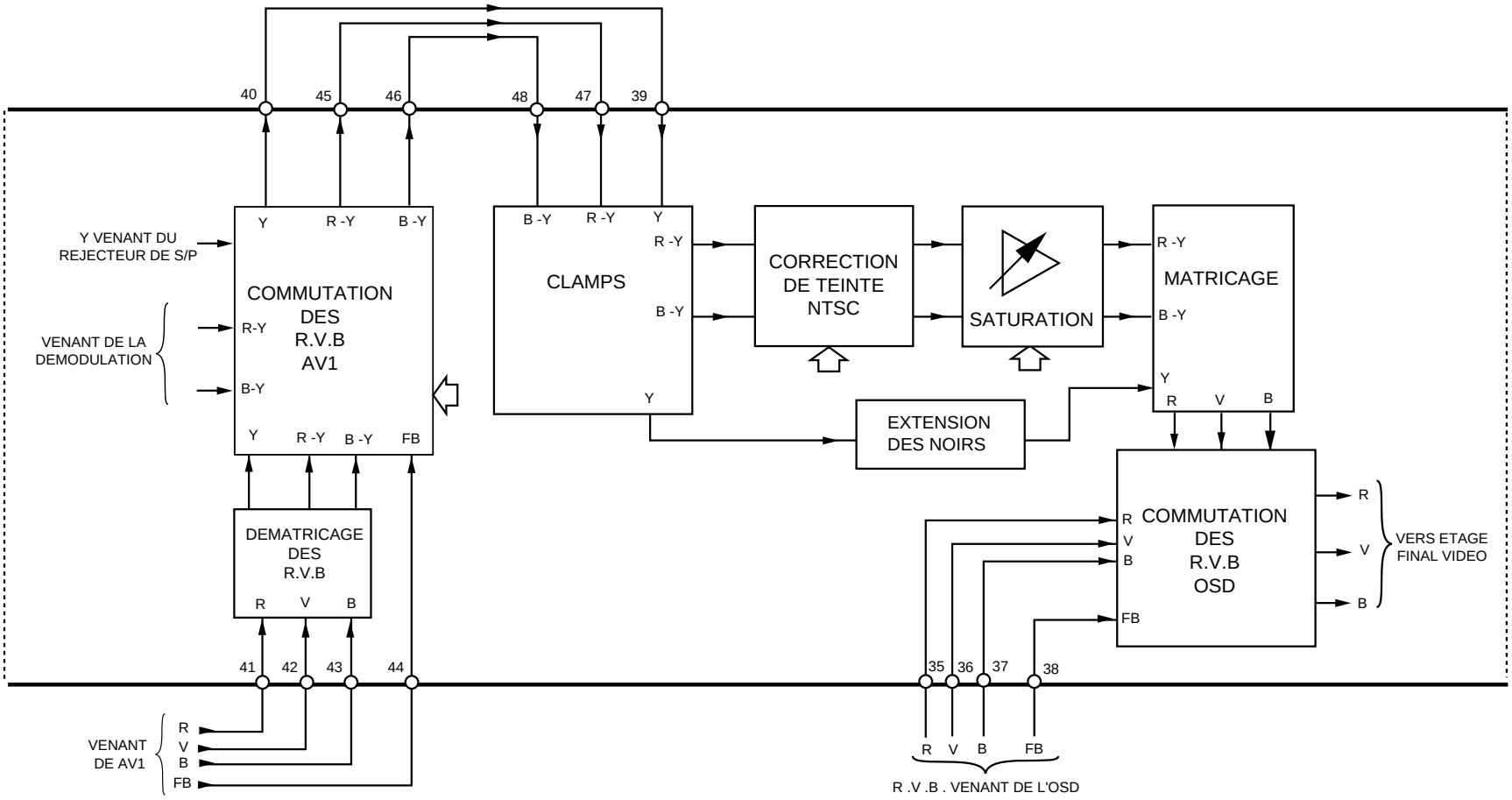
CHROMA IDENTIFICATION

In IV01, the separated video or chroma signals are directed to the input chroma filter (bell or bandwidth), the accord of this filter is adjusted automatically by a PLL loop accorded for PAL and NTSC by the 3.58 or 4.43 MHz oscillators or for SECAM by the B-Y demodulator at 4.250 MHz.
This decoder is multi-standard and can identify all known standards (PAL 4.43, PAL 3.58, SECAM, NTSC 4.43, NTSC 3.58). Only two quartzes and a loop filter are external to the integrated circuit. Identification of the standard is automatic but can be forced by the I2C bus.


CC
10
SECAM
PLL
28
S/P+N
DEMODULATION
SECAM
SECAM
DISCRIMINATEUR ROUGE
DISCRIMINATEUR BLEU
VIENT DE
L'IDENTIFICATION
DE STANDARD
RETARD 64 µs
R -Y
VERS
COMMUTATION
R .V .B
DEMODULATION
PAL/NTSC
PAL
DEMODULATEUR ROUGE
DEMODULATEUR BLEU
RETARD 64 µs
B -Y
50
51
52
3,58
MHZ
4,43
MHZ
CC
05
RC
05
CC
04
QC02
FILTRE DE
BOUCLE

CHROMA DEMODULATION

The identified chroma signals are applied towards demodulators R-Y and B-Y. In PAL and NTSC there are two synchronous demodulators controlled by the 4.43 or 3.58 MHz oscillator. In SECAM the signals R-Y and B-Y cross two delay lines of 64 ms for SECAM permutation prior to application at the switching circuit.



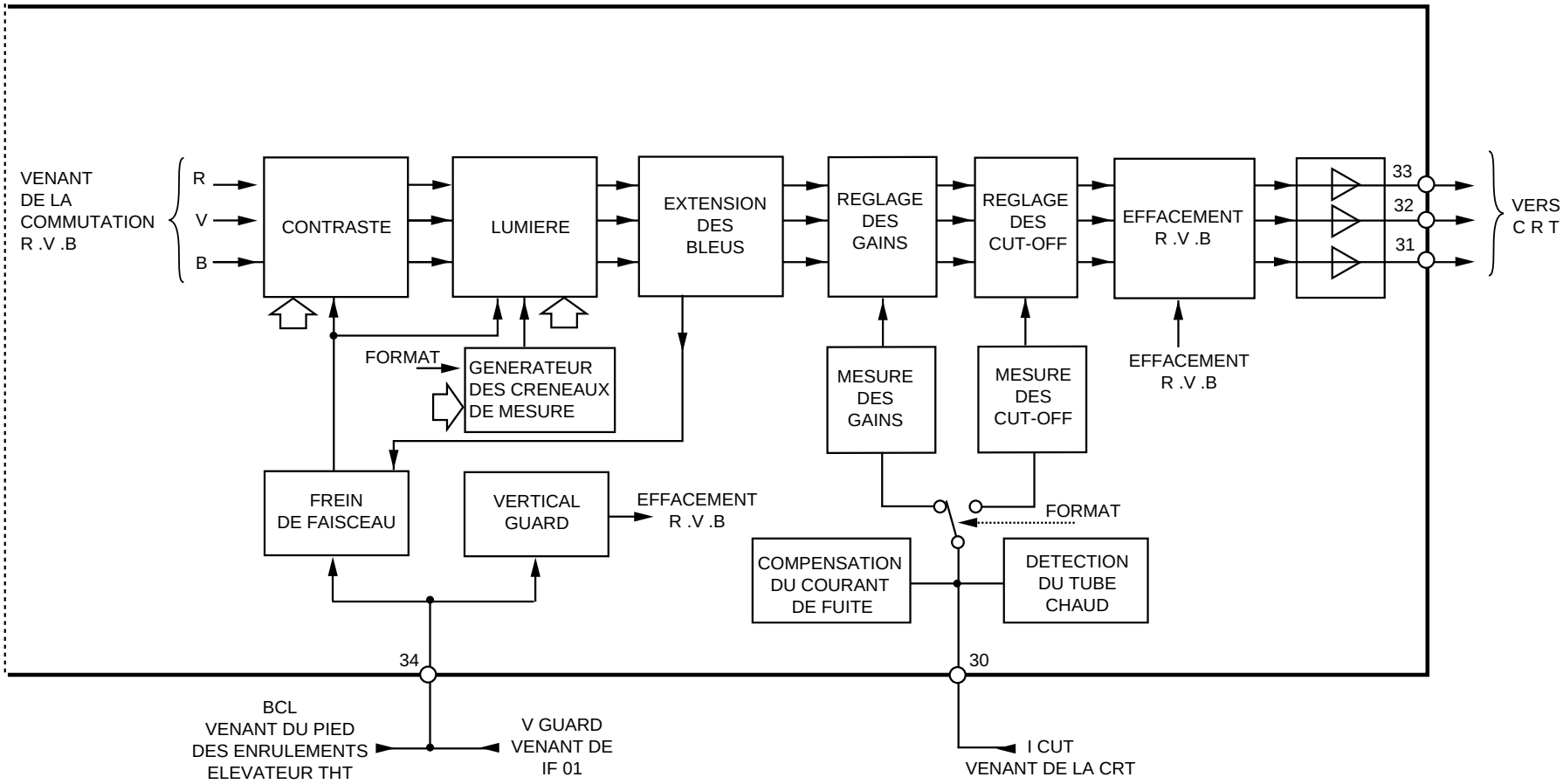
THOMSON MULTI MEDIA

CENTRE DE FORMATION TECHNIQUE

SWITCHING OF RGB, AV1 AND OSD

The signals Y, R-Y, B-Y are fed to the first switching input, the dematrixed R, G, B from the AVI SCART connector (pins 41, 42, 43) are present at the second input, the FB fast switching signal (pin 44) makes the selection between the two sources.
The switched signals leave the integrated circuit pins 40, 45, 46 and are fed to pins 48, 47, 39.
After a clamp stage followed by NTSC shade correction and chroma saturation they are RGB matrixed.

The RGB are again switched with the RGB from the OSD pins 35, 36, 37, the rapid switching signal at pin 38 making the selection.
The switched RGB signals are sent to the final video stage.


VENANT
DE LA
COMMUTATION
R .V .B
R
V
B
CONTRASTE
LUMIERE
EXTENSION
DES
BLEUS
REGLAGE
DES
GAINS
REGLAGE
DES
CUT-OFF
EFFACEMENT
R .V .B
33
32
31
VERS
C R T
FORMAT
GENERATEUR
DES CRENEAUX
DE MESURE
MESURE
DES
GAINS
MESURE
DES
CUT-OFF
EFFACEMENT
R .V .B
FREIN
DE FAISCEAU
VERTICAL
GUARD
EFFACEMENT
R .V .B
FORMAT
COMPENSATION
DU COURANT
DE FUITE
DETECTION
DU TUBE
CHAUD
34
30
BCL
VENANT DU PIED
DES ENRULEMENTS
ELEVATEUR THT
V GUARD
VENANT DE
IF 01
I CUT
VENANT DE LA CRT

RGB PROCESSING

The selected signals are adjusted for light/contrast. The beam brake data from pin 34 is received at the light and contrast adjustment stages. This data, originating from the base of the THT elevator windings, indicates the tube rate.
The "VERTICAL GUARD" signal allows, in the case of frame failure, cutting off the three channels to avoid burning the tube.
The blues extension circuit allows reducing the red and green when the image becomes very luminous.
Slaving of the tube to the black and white levels is performed by the intermediary of the ICUT data pin 30, such data also allowing indicating to the integrated circuit that the tube is warm.
After the RVB amplification and deletion circuits the signals are output from pins 31, 23 and 33 towards the CRT.

R G B
AMPLIFIER

CONTENTS

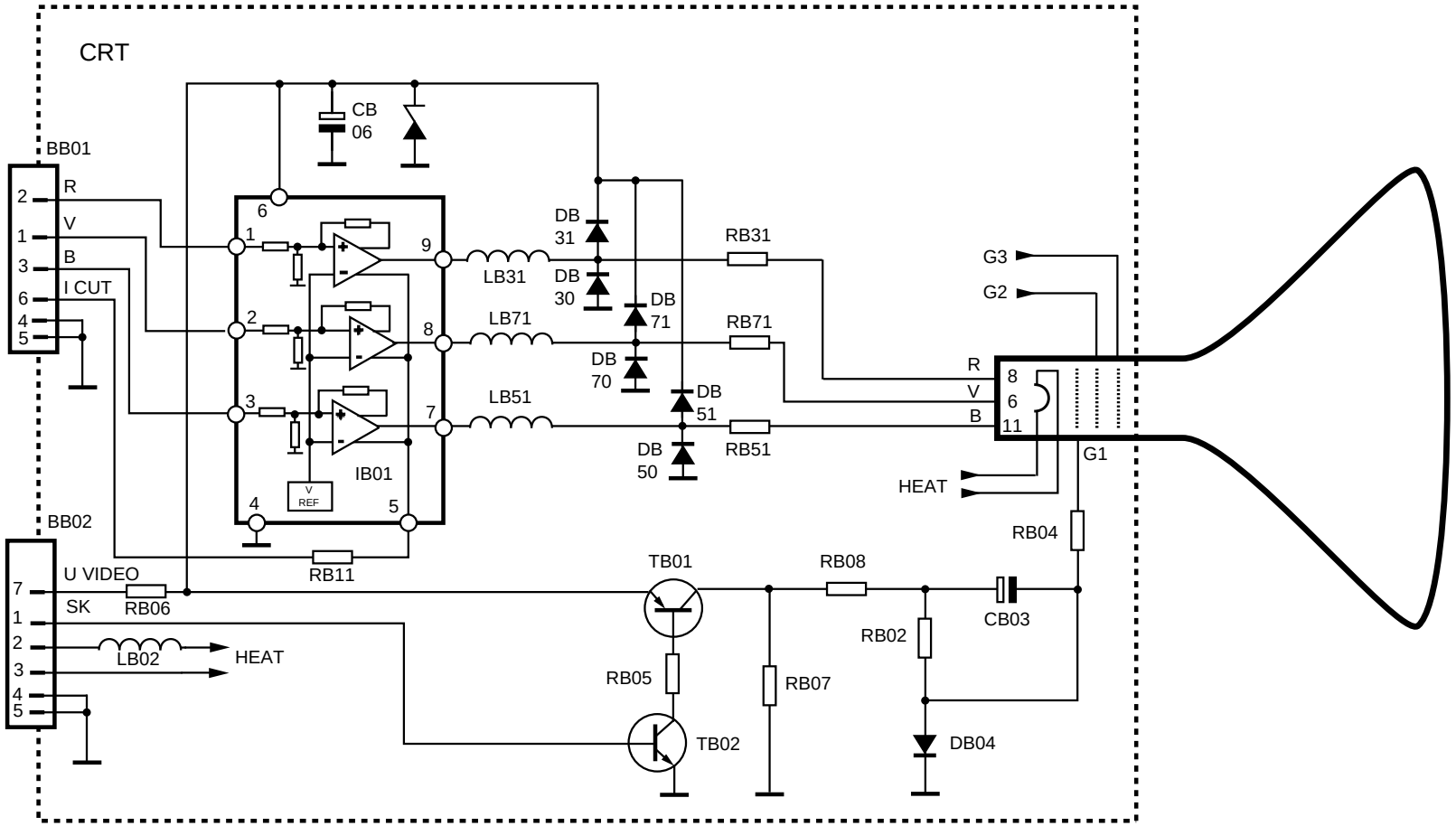
GENERAL

RGB AMPLIFIER

SPOT BLOWING

THOMSON MULTI MEDIA

CENTRE DE FORMATION TECHNIQUE


CRT
CB
06
BB01
2
1
3
6
4
5
R
V
B
I CUT
6
1
2
3
9
8
7
4
5
IB01
V
REF
LB31
LB71
LB51
DB
31
DB
30
DB
71
DB
70
DB
51
DB
50
RB31
RB71
RB51
G3
G2
R
V
B
8
6
11
G1
HEAT
RB04
BB02
7
1
2
3
4
5
U VIDEO
SK
RB06
RB11
LB02
HEAT
TB01
RB08
CB03
RB02
RB05
RB07
TB02
DB04

GENERAL

RGB amplification is performed by circuit IB01 TDA 6107Q. This circuit is based on the same concept as circuit IV01 TDA 8855, that is with the minimum of external components.

RGB AMPLIFIER

This circuit is composed of three independent amplifiers. It is supplied with power by the U VIDEO 200 V at pin 6, the polarisation voltages and gain are obtained through resistors and an internal reference voltage generator. RGB are present at pins 1, 2 and 3 and the amplified RGB exit via pins 7, 8 and 9.

SPOT BLOWING

When the TV set is in use, the transistors TB01 and TB02 are saturated, the capacitor is charged at the supply voltage, that is 200 V, G1 is polarised at 0.7 V by diode DB04.
When the TV set is switched off, the signal SK from µC IR01 blocks transistors TB01 and TB02, capacitor CB04 discharges via RB02 causing blocking of DB04 and applying a negative voltage to G1.S

AUDIO PROCESSING

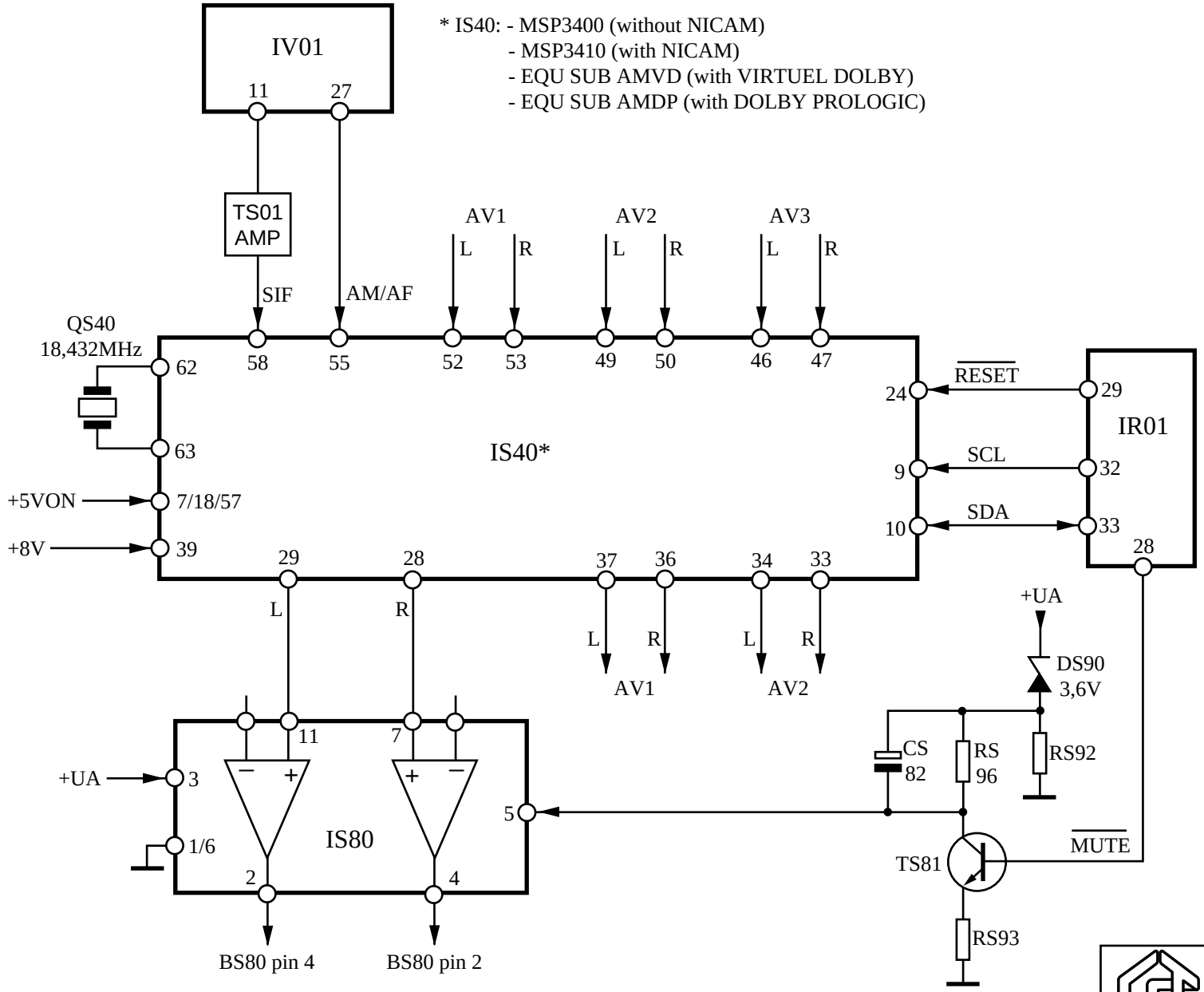
CONTENTS

AUDIO MODULE WITH MSP34XX

AUDIO MODULE WITH EQU SUB AMVD

AUDIO MODULE WITH EQU SUB AMDP

POWER AMPLIFIER (DOLBY VERSION)


* IS40: - MSP3400 (without NICAM)
- MSP3410 (with NICAM)
- EQU SUB AMVD (with VIRTUEL DOLBY)
- EQU SUB AMDP (with DOLBY PROLOGIC)
IV01
11
27
TS01
AMP
SIF
AM/AF
AV1
AV2
AV3
L
R
QS40
18,432MHz
62
63
+5VON
7/18/57
+8V
39
58
55
52
53
49
50
46
47
IS40*
24
9
10
RESET
SCL
SDA
29
32
33
28
IR01
29
28
37
36
34
33
L
R
AV1
AV2
+UA
DS90
3,6V
CS
82
RS
96
RS92
11
7
+UA
3
1/6
IS80
5
2
4
TS81
MUTE
RS93
BS80 pin 4
BS80 pin 2

82

AUDIO MODULE WITH MSP34XX

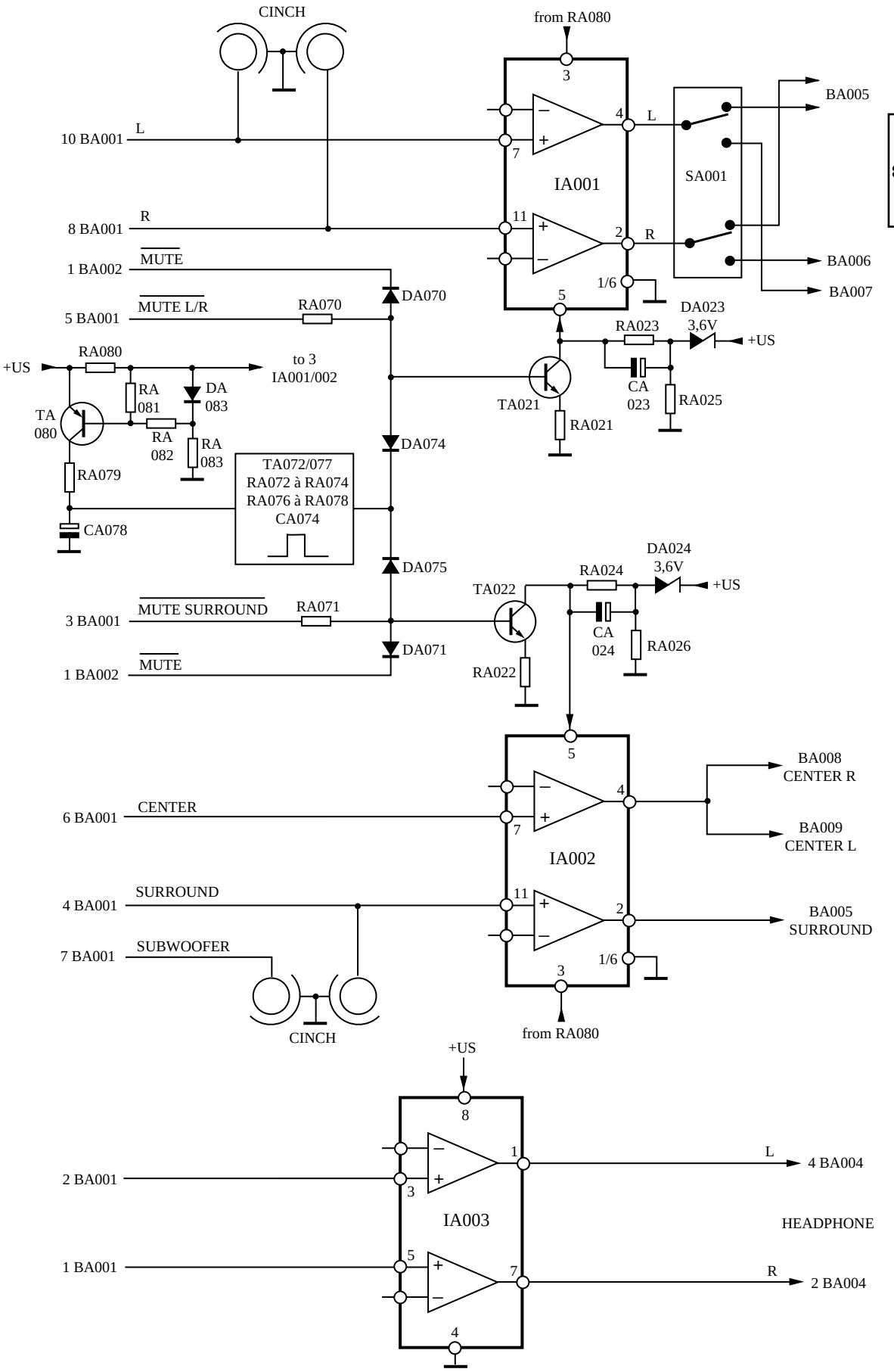
The integrated circuit IS40 (MSP3400 or MSP3410) is used for audio processing. It is managed by an 18.432 MHz clock. The management µC, IR01, controls it via the IIC bus and executes reset via pin 29.

The circuit performs :
- Demodulation of the audio FM intermediary carriers
- Demodulation of the NICAM audio (MSP3410 only)
- Switching of the various analogue audio sources for the SCART outputs
- Analogue/digital conversion of the various audio sources
- Correction of the digital audio signals (tone, pseudo stereo, extended stereo, volume, etc.)
- Digital/analogue conversion.

The audio signals for the hps outputs are available on pins 28 and 29 of IS40. They are sent to the power amplifier IS80.
The transistor TS81 and its associated components, controlled by output 28 of IR01, supply audio mute during :
- Changing of channels
- Searching for a transmitter
- Cutting off the sound (silence key)
- Starting up the TV set when the tube is not warm
- Switching off the TV set
- The stand by and timer functions.

AUDIO MODULE WITH EQU SUB AMVD
AUDIO MODULE WITH EQU SUB AMDP

The circuit EQU SUB AMVD incorporates two integrated circuits, 1 MSP3410D and 1 DPL3518A.


CINCH
from RA080
3
10 BA001
L
7
IA001
4
L
BA005
SA001
8 BA001
R
11
2
R
BA006
BA007
1 BA002
MUTE
1/6
5
5 BA001
MUTE L/R
RA070
DA070
DA023
3,6V
RA023
+US
RA080
+US
to 3
IA001/002
TA
080
RA
081
DA
083
RA
082
RA
083
RA079
TA021
RA021
CA
023
RA025
DA074
TA072/077
RA072 à RA074
RA076 à RA078
CA074
CA078
DA075
DA024
3,6V
RA024
+US
TA022
3 BA001
MUTE SURROUND
RA071
CA
024
RA026
DA071
1 BA002
MUTE
RA022
5
BA008
CENTER R
4
6 BA001
CENTER
7
IA002
BA009
CENTER L
SURROUND
4 BA001
11
2
BA005
SURROUND
7 BA001
SUBWOOFER
1/6
3
CINCH
from RA080
+US
8
1
L
4 BA004
2 BA001
3
IA003
HEADPHONE
5
1 BA001
7
R
2 BA004
4

POWER AMPLIFIER (DOLBY VERSION)

IA001 amplifies the power for the left and right hps
IA002 amplifies the power for the centre and surround hps

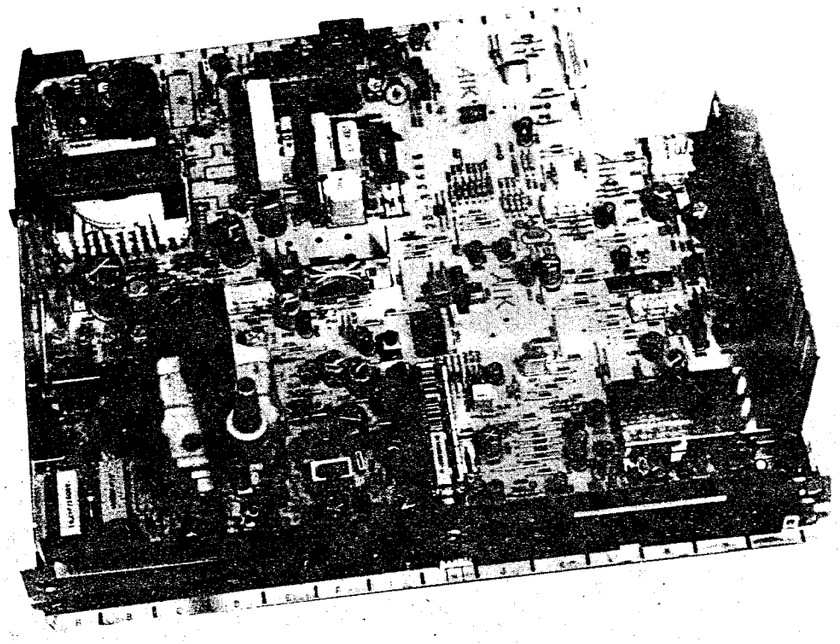
A measurement of the current supplying the integrated circuits IA001 and IA002 is made via RA080 and TA080. In the case of overload, TA080 is saturated and triggers the audio mute, via the monostable TA072/TA077.

THOMSON MULTI MEDIA

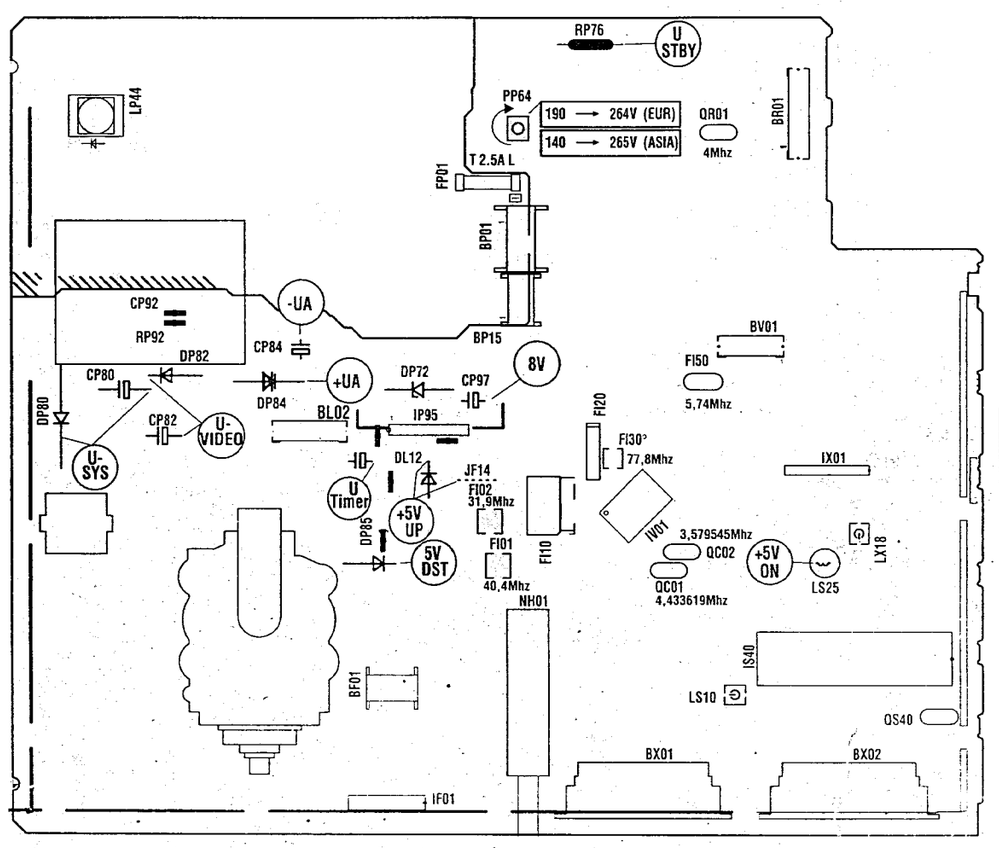
Brandt FERGUSON **NORDMENDE** SABA **TELEFUNKEN** THOMSON

TV

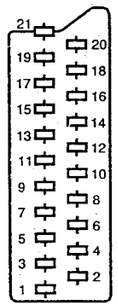
ICC17



LOCATION OF CONTROLS - EMPLACEMENT DES REGLAGES - SERVICE LAGEPLAN - POSIZIONE REGOLATORI DI SERVIZIO - SITUACIÓN DE LOS AJUSTES



* it is not necessary , to adjust FI30 by after sales



NOTE : (MAIN) ... etc. identifies each pcb module.

NOTE : (MAIN) ... etc. repères des platines constituant l'appareil.

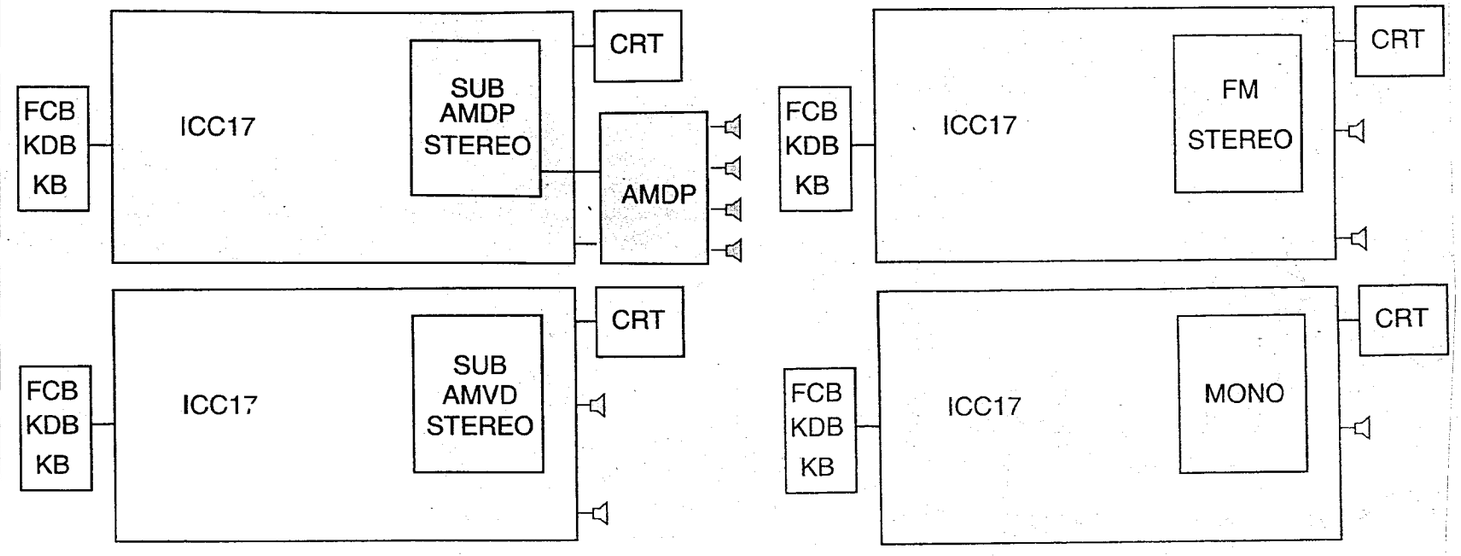
HINWEIS : (MAIN) ... usw. Kennzeichnung der Platinen, aus denen das Gerät zusammengesetzt ist.

NOTA : (MAIN) ... ecc. indicazioni delle piastre che costituiscono l'apparecchio.

NOTA : (MAIN) ... etc. marcas de las placas que constituyen el aparato.

		ENGLISH	FRANÇAIS	DEUTSCH	ITALIANO	ESPAÑOL
1	⊖→	AUDIO "R"	AUDIO "D"	AUDIO "R"	AUDIO "D"	AUDIO "D"
2	→⊕	AUDIO "R"	AUDIO "D"	AUDIO "R"	AUDIO "D"	AUDIO "D"
3	⊖→	AUDIO "L"	AUDIO "G"	AUDIO "L"	AUDIO "S"	AUDIO "I"
4	⊥	AUDIO	AUDIO	AUDIO	AUDIO	AUDIO
5	—	"BLUE"	"BLEU"	"BLAU"	"BLU"	"AZUL"
6	→⊕	AUDIO "L" MONO	AUDIO "G" MONO	AUDIO "L" MONO	AUDIO "S" MONO	AUDIC "I" MONO
7	→⊕	"BLUE"	"BLEU"	"BLAU"	BLU	AZUL
8	→⊕	SLOW SWITCH	COMMUT. LENTE	AV UMSCHALTUNG	"COMMUTAZIONE LENTA"	"CONMUTACION LENTA"
9	—	"GREEN"	"VERT"	"GRÜN"	"VERDE"	"VERDE"
10	NC					
11	→⊕	"GREEN"	"VERT"	"GRÜN"	"VERDE"	"VERDE"
12	NC					
13	—	"RED"	"ROUGE"	"ROT"	"ROSSO"	"ROJA"
14	NC					
15	→⊕	"RED"	"ROUGE"	"ROT"	"ROSSO"	"ROJA"
16	→⊕	FAST SWITCH	COMMUT. RAPIDE	AUSTASTUNG	"COMMUTAZIONE RAPIDA"	"CONMUTACION RAPIDA"
17	⊥	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO
18	⊥	FAST SWITCH	COMMUT. RAPIDE	AUSTASTUNG	"COMMUTAZIONE RAPIDA"	"CONMUTACION RAPIDA"
19	⊖→	VIDEO	VIDEO	VIDEO	VIDEO	VIDEO
20	→⊕	VIDEO OR "SYNC"	VIDEO SYNCHRO	VIDEO ODER SYNCHRO	VIDEO O SINCRO	VIDEO O SINCRO
21	⊖→	PLUG SCREEN BOX	BLINDAGE PRISE	ABSCHIRMUNG DES STECKERS	ARMATURA DELLA SPINA	BLINDAJE DEL ENCHUFE

→⊕ : INPUT - ENTRÉE - EINGANG - ENTRATA - ENTRADA • ⊖→ : OUTPUT - SORTIE - AUSGANG - USCITA - SALIDA • ⊥ : EARTH - MASSE - MASSE - MASSA - MASA



(5) : standby

Note :
During measurements in the power supply unit
- Use the primary power unit ground (PGND).

Attention :
Mesure dans le bloc alimentation
- Utiliser la masse du bloc alimentation (PGND).

Achtung :
Bei Messungen im Primärnetzteil
- Primärnetzteilmasse verwenden (PGND).

Attenzione :
misure nell'alimentatore primario
- usare massa alimentazione primario (PGND).

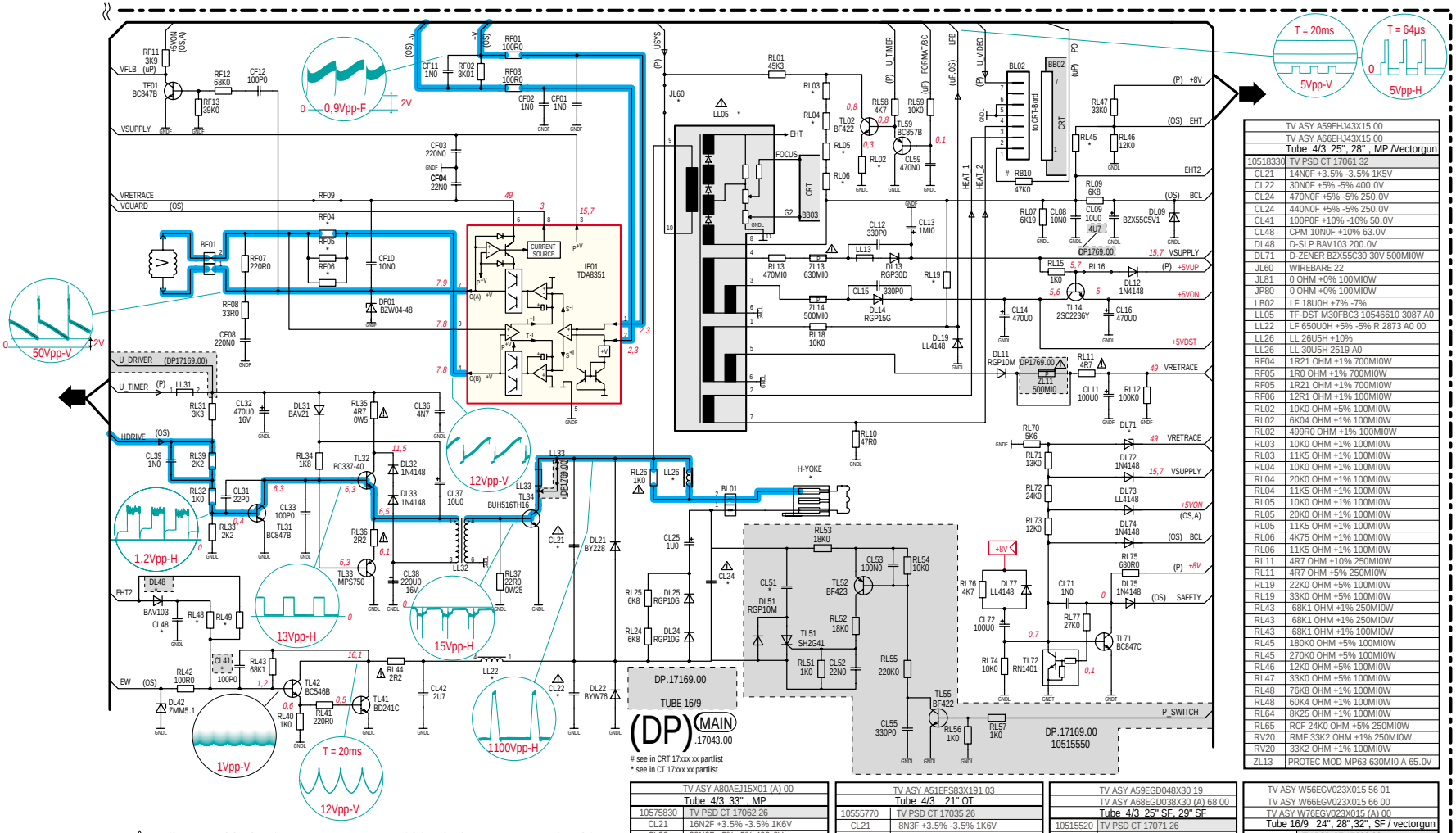
Cuidado :
Medida en el bloque de alimentacion
- Utilizar la masa del bloque de alimentacion (PGND).

Part of board connected to mains supply.
Partie du châssis reliée au secteur.
Primärseite des Netzteils.
Parte dello châssis collegata alla rete.
Parte del chassis conectar a la red.

MAIN (PP)17900

Tube	Format	Usys	Jumper	RL65
A51EFS83X191	4:3	126V	JL80	4k7
A59EHJ43X15	4:3	132V	JL81	24k
A66EHJ43X15	4:3	132V	JL81	24k
A59EGD048X30	4:3	126V	JL80	4k7
A68EGD038X30	4:3	126V	JL80	4k7
A68AGA25X01	4:3	126V	JL80	4k7
A80AEJ15X01	4:3	126V	JL80	4k7
W56EGV023X015	16:9	138V	JL82	47k
W66EGV023X015	16:9	138V	JL82	47k
W76EGV023X015	16:9	138V	JL82	47k

Use isolating mains transformer - Utiliser un transformateur isolateur du secteur -Einen Trenntrafo verwenden
Utilizar un transformador aislador de red - Utilizzare un trasformatore per isolarvi dalla rete



TV ASY A59EHJ43X15 00
TV ASY A66EHJ43X15 00
Tube 4/3 25", 28" , MP /Vectorgun
10518330	TV PSD CT 17061 32
CL21	14N0F +3.5% -3.5% 1K5V
CL22	30N0F +5% -5% 400.0V
CL24	470N0F +5% -5% 250.0V
CL24	440N0F +5% -5% 250.0V
CL41	100P0F +10% -10% 50.0V
CL48	CPM 10N0F +10% 63.0V
DL48	D-SLP BAV103 200.0V
DL71	D-ZENER BZX55C30 30V 500MI0W
JL60	WIREBARE 22
JL81	0 OHM +0% 100MI0W
JP80	0 OHM +0% 100MI0W
LB02	LF 18U0H +7% -7%
LL05	TF-DST M30FBC3 10546610 3087 A0
LL22	LF 650U0H +5% -5% R 2873 A0 00
LL26	LL 26U5H +10%
LL26	LL 30U5H 2519 A0
RF04	1R21 OHM +1% 700MI0W
RF05	1R0 OHM +1% 700MI0W
RF05	1R21 OHM +1% 700MI0W
RF06	12R1 OHM +1% 100MI0W
RL02	10K0 OHM +5% 100MI0W
RL02	6K04 OHM +1% 100MI0W
RL02	499R0 OHM +1% 100MI0W
RL03	10K0 OHM +1% 100MI0W
RL03	11K5 OHM +1% 100MI0W
RL04	10K0 OHM +1% 100MI0W
RL04	20K0 OHM +1% 100MI0W
RL04	11K5 OHM +1% 100MI0W
RL05	10K0 OHM +1% 100MI0W
RL05	20K0 OHM +1% 100MI0W
RL05	11K5 OHM +1% 100MI0W
RL06	4K75 OHM +1% 100MI0W
RL06	11K5 OHM +1% 100MI0W
RL11	4R7 OHM +10% 250MI0W
RL11	4R7 OHM +5% 250MI0W
RL19	22K0 OHM +5% 100MI0W
RL19	33K0 OHM +5% 100MI0W
RL43	68K1 OHM +1% 250MI0W
RL43	68K1 OHM +1% 250MI0W
RL43	68K1 OHM +1% 100MI0W
RL45	180K0 OHM +5% 100MI0W
RL45	270K0 OHM +5% 100MI0W
RL46	12K0 OHM +5% 100MI0W
RL47	33K0 OHM +5% 100MI0W
RL48	76K8 OHM +1% 100MI0W
RL48	60K4 OHM +1% 100MI0W
RL64	8K25 OHM +1% 100MI0W
RL65	RCF 24K0 OHM +5% 250MI0W
RV20	RMF 33K2 OHM +1% 250MI0W
RV20	33K2 OHM +1% 100MI0W
ZL13	PROTEC MOD MP63 630MI0 A 65.0V

TV ASY A80AEJ15X01 (A) 00
Tube 4/3 33" , MP
10575830	TV PSD CT 17062 26
CL21	16N2F +3.5% -3.5% 1K6V
CL22	30N0F +5% -5% 400.0V
CL24	560N0F +5% -5% 250.0V
CL41	100P0F +10% -10% 50.0V
CL48	10N0F +10% 63.0V
DL48	D-SLP BAV103 200.0V
DL71	D-ZENER BZX55C30 30V 500MI0W
JL60	WIREBARE 22
JL80	0 OHM +0% 100MI0W
LB02	LF 32U0H +4% -4%
LL05	TF-DST TDS29 TBD 11
LL22	LF 650U0H +5% -5% R 2873 A0 00
LL26	LL 26U5H +10%
RF05	1R21 OHM +1% 700MI0W
RF06	10R0 OHM +1% 100MI0W
RL02	6K04 OHM +1% 100MI0W
RL03	4K75 OHM +1% 100MI0W
RL04	4K75 OHM +1% 100MI0W
RL05	4K75 OHM +1% 100MI0W
RL06	6K81 OHM +1% 100MI0W
RL19	13K0 OHM +5% 100MI0W
RL45	150K0 OHM +5% 100MI0W
RL48	76K8 OHM +1% 100MI0W
RL49	560K0 OHM +5% 100MI0W
RL65	RCF 4K7 OHM +5% 250MI0W
RV20	RMF 23K7 OHM +1% 250MI0W

TV ASY A51EFS83X191 03
Tube 4/3 21" OT
10555770	TV PSD CT 17035 26
CL21	8N3F +3.5% -3.5% 1K6V
CL22	33N0F +5% -5% 1K0V
CL24	440N0F +5% -5% 250.0V
CL41	1N0F +10% -10% 50.0V
DL71	D-ZENER BZX55C24 24V 500MI0W
JL60	WIREBARE 22
JL80	0 OHM +0% 100MI0W
LB02	LF 18U0H +7% -7%
LL05	TF-DST M30FBC3 10555640 3087 A0
LL22	LF 650U0H +5% -5% R 2873 A0 00
LL26	LL 85U0H 2519 A0
RF05	1R5 OHM +1% 700MI0W
RF06	10R0 OHM +1% 100MI0W
RL02	6K04 OHM +1% 100MI0W
RL03	10K0 OHM +1% 100MI0W
RL04	10K0 OHM +1% 100MI0W
RL05	10K0 OHM +1% 100MI0W
RL06	3K32 OHM +1% 100MI0W
RL45	110K0 OHM +5% 100MI0W
RL49	60K4 OHM +1% 100MI0W
RL65	4K7 OHM +5% 250MI0W
RV20	23K7 OHM +1% 250MI0W

TV ASY A59EGD048X30 19
TV ASY A68EGD038X30 (A) 68 00
Tube 4/3 25" SF, 29" SF
10515520	TV PSD CT 17071 26
CL21	16N2F +3.5% -3.5% 1K6V
CL22	30N0F +5% -5% 400.0V
CL24	510N0F +5% -5% 250.0V
CL41	100P0F +10% -10% 50.0V
CL48	10N0F +10% 63.0V
DL48	D-SLP BAV103 200.0V
DL71	D-ZENER BZX55C30 30V 500MI0W
JL60	WIREBARE 22
JL80	0 OHM +0% 100MI0W
LB02	LF 32U0H +4% -4%
LL05	TF-DST TDS29 TBD 13
LL22	LF 650U0H +5% -5%
LL26	LL 26U5H +10%
RF05	RMF 1R0 OHM +1% 700MI0W
RL02	6K8 OHM +5% 100MI0W
RL03	4K75 OHM +1% 100MI0W
RL04	4K75 OHM +1% 100MI0W
RL05	4K75 OHM +1% 100MI0W
RL06	4K75 OHM +1% 100MI0W
RL19	15K0 OHM +5% 100MI0W
RL45	180K0 OHM +5% 100MI0W
RL48	100K0 OHM +5% 100MI0W
RL49	300K0 OHM +5% 100MI0W
RL65	4K7 OHM +5% 250MI0W
RV20	33K2 OHM +1% 250MI0W

TV ASY W56EGV023X015 56 01
TV ASY W66EGV023X015 66 00
TV ASY W76EGV023X015 (A) 00
Tube 16/9 24", 28",32", SF / vectorgun
10515530	TV PSD CT 17083 38
CL21	15N5F +3.5% -3.5% 1K6V
CL22	27N0F +5% -5% 400.0V
CL24	440N0F +5% -5% 250.0V
CL41	100P0F +10% -10% 50.0V
CL48	100N0F +5% 63.0V
CL51	290N0F +5% -5% 250.0V
DL48	D-SLP BAV103 200.0V
DL71	D-ZENER BZX55C24 24V 500MI0W
JL60	WIREBARE 22
JL80	0 OHM +0% 100MI0W
LB02	LF 32U0H +4% -4%
LL05	TF-DST TDS29 15314460 10
LL22	LF 650U0H +5% -5%
LL26	LL 30U5H 2519 A0
RF05	1R21 OHM +1% 700MI0W
RL02	4K99 OHM +1% 100MI0W
RL03	6K49 OHM +1% 100MI0W
RL04	6K49 OHM +1% 100MI0W
RL05	6K49 OHM +1% 100MI0W
RL06	2K37 OHM +1% 100MI0W
RL19	13K0 OHM +5% 100MI0W
RL45	390K0 OHM +5% 100MI0W
RL48	220K0 OHM +5% 100MI0W
RL49	180K0 OHM +5% 100MI0W
RL65	47K0 OHM +5% 250MI0W
RV20	100K0 OHM +1% 250MI0W

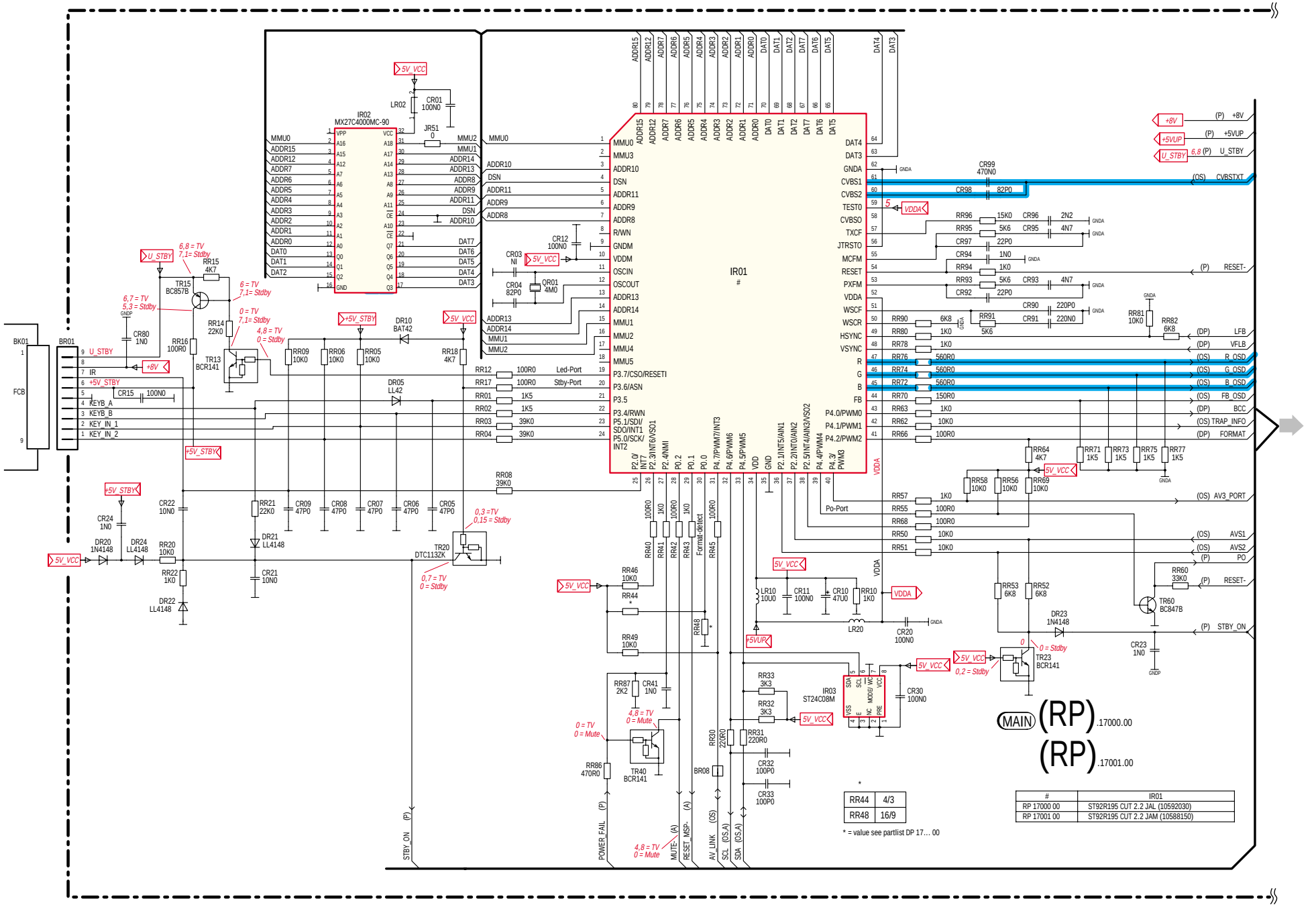
⚠ Indicates critical safety components, and identical components should be used for replacement. Only then can the operational safety be garanteed.

Le remplacement des éléments de sécurité (repérés avec le symbole ⚠) par des composants non homologués selon la Norme CEI 65 entraine la non-conformité de l'appareil.
Dans ce cas, la responsabilité du fabricant n'est plus engagée.

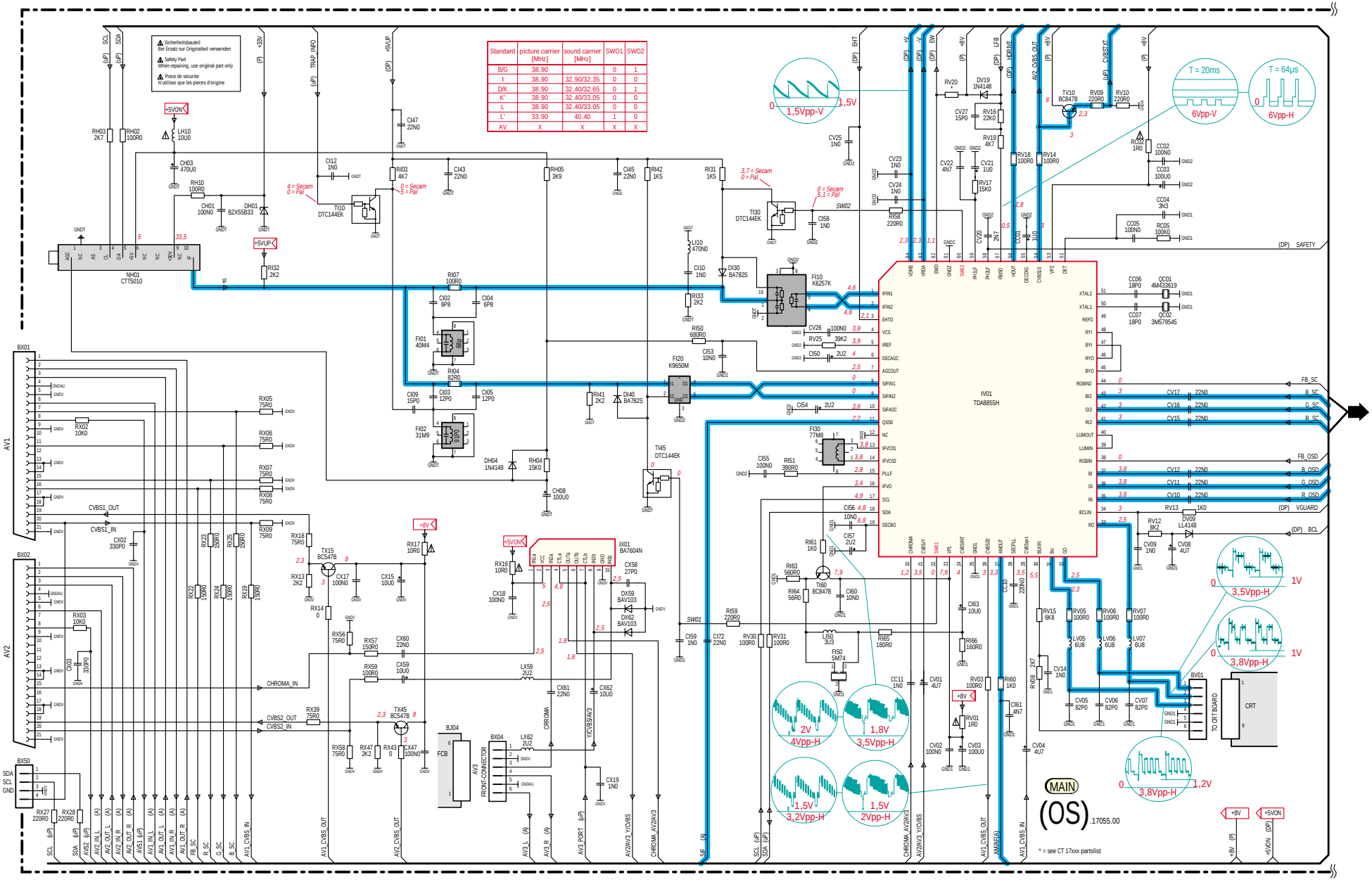
Wenn Sicherheitsteile (mit dem Symbol ⚠ gekennzeichnet) durch nicht normgerechte Teile ersetzt werden, erlischt die Haftung des Herstellers.

La sostituzione degli elementi di sicurezza (contrassegnati con il segno ⚠) con componenti non omologati secondo la norma CEI 65 comporta la non conformitá dell'apparecchio.
In tal caso é "esclusa la responsabilità" del costruttore.

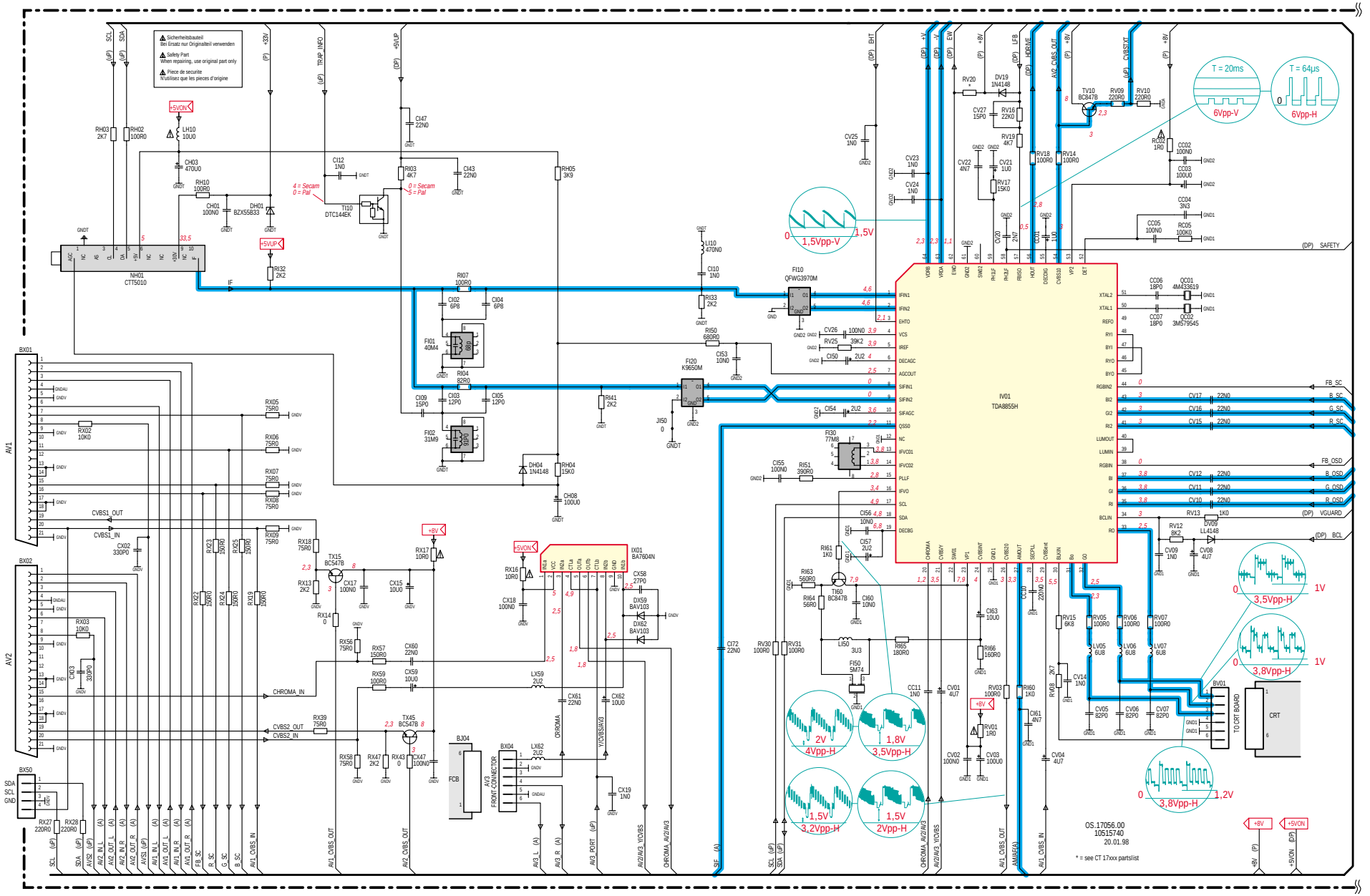
La subtitución de elementos de seguridad (marcados con el simbolo ⚠) por componentes no homologados segun la norma CEI 65, provoca la no conformidad del aparato.
En ese caso, el fabricante cesa de ser responsable.


IR01
IR02 MX27C4000MC-90
IR03 ST24C08M
BK01
BR01
FCB
TR15 BC857B
TR13 BCR141
TR20 DTC113ZK
TR40 BCR141
TR23 BCR141
TR60 BC847B
DR10 BAT42
DR05 LL42
DR20 1N4148
DR24 LL4148
DR21 LL4148
DR22 LL4148
DR23 1N4148
+8V
+5V_STBY
5V_VCC
U_STBY
VDDA
+5VUP
GNDA
GNDP
Led-Port
Stby-Port
Format-detect
Po-Port
POWER_FAIL (P)
STBY_ON (P)
MUTE (A)
RESET_MSP- (A)
AV_LINK (OS)
SCL (OS,A)
SDA (OS,A)
(OS) CVBSTXT
(DP) LFB
(DP) VFLB
(OS) R_OSD
(OS) G_OSD
(OS) B_OSD
(OS) FB_OSD
(DP) BCC
(OS) TRAP_INFO
(DP) FORMAT
(OS) AV3_PORT
(OS) AVS1
(OS) AVS2
(P) PO
(P) RESET-
(P) STBY_ON
MAIN (RP).17000.00
(RP).17001.00
RR44 4/3
RR48 16/9
* = value see partlist DP 17... 00
# IR01
RP 17000 00 ST92R195 CUT 2.2 JAL (10592030)
RP 17001 00 ST92R195 CUT 2.2 JAM (10588150)

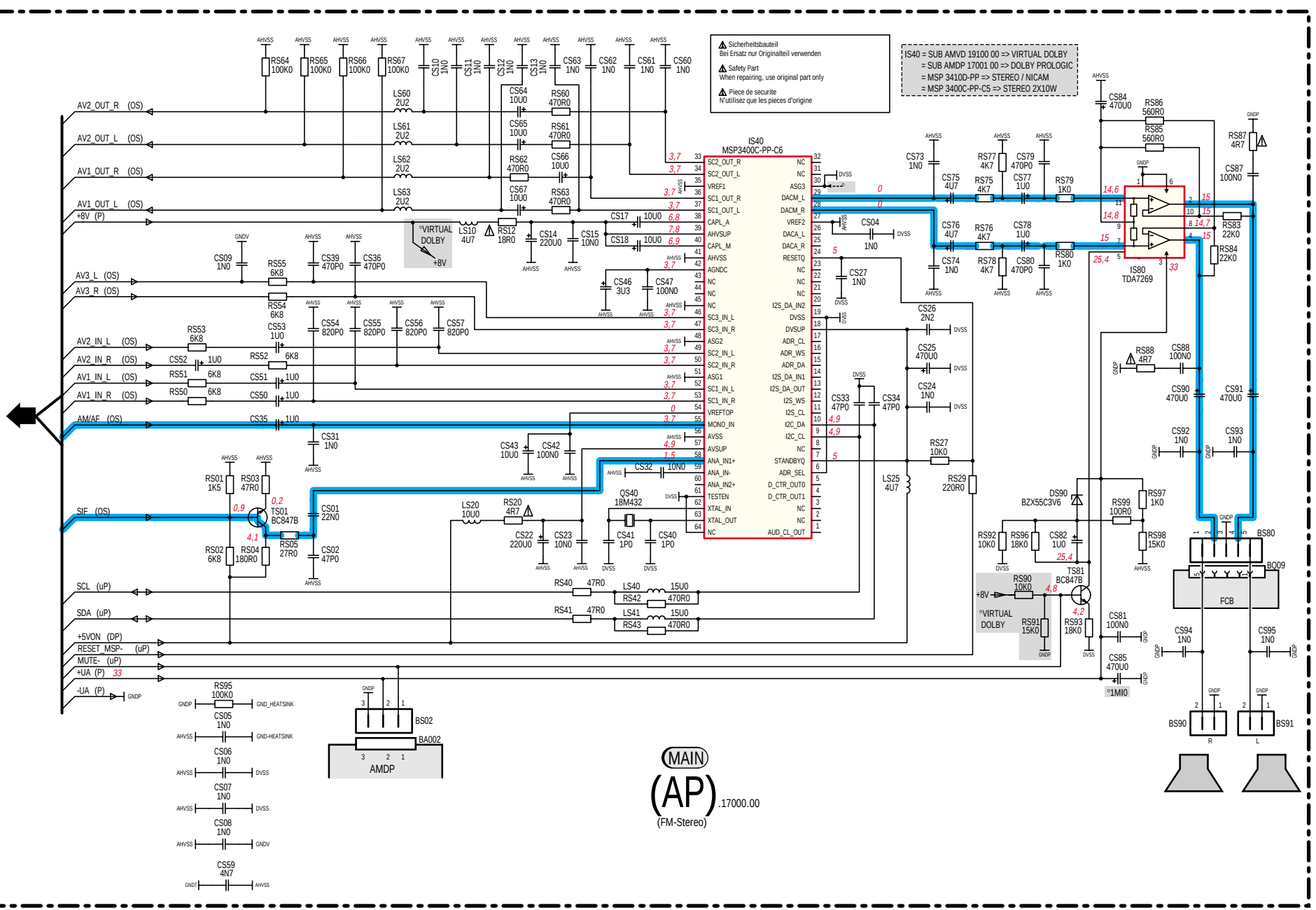
RF/FI/ SCART INTERFACE/VIDEO SIGNAL PROCESSING -HF/FI INTERFACE PERITELEVISION/TRAITEMENT LUMINANCE CHROMINANCE - HF/ZF/ SCART INTERFACE/VIDEO SIGNALVERARBEITUNG - RF/FI /PRESA PERITEL/ELABORAZIONE VIDEO - RF/FI /EUROCONECTOR / TRATAMENTO VIDEO



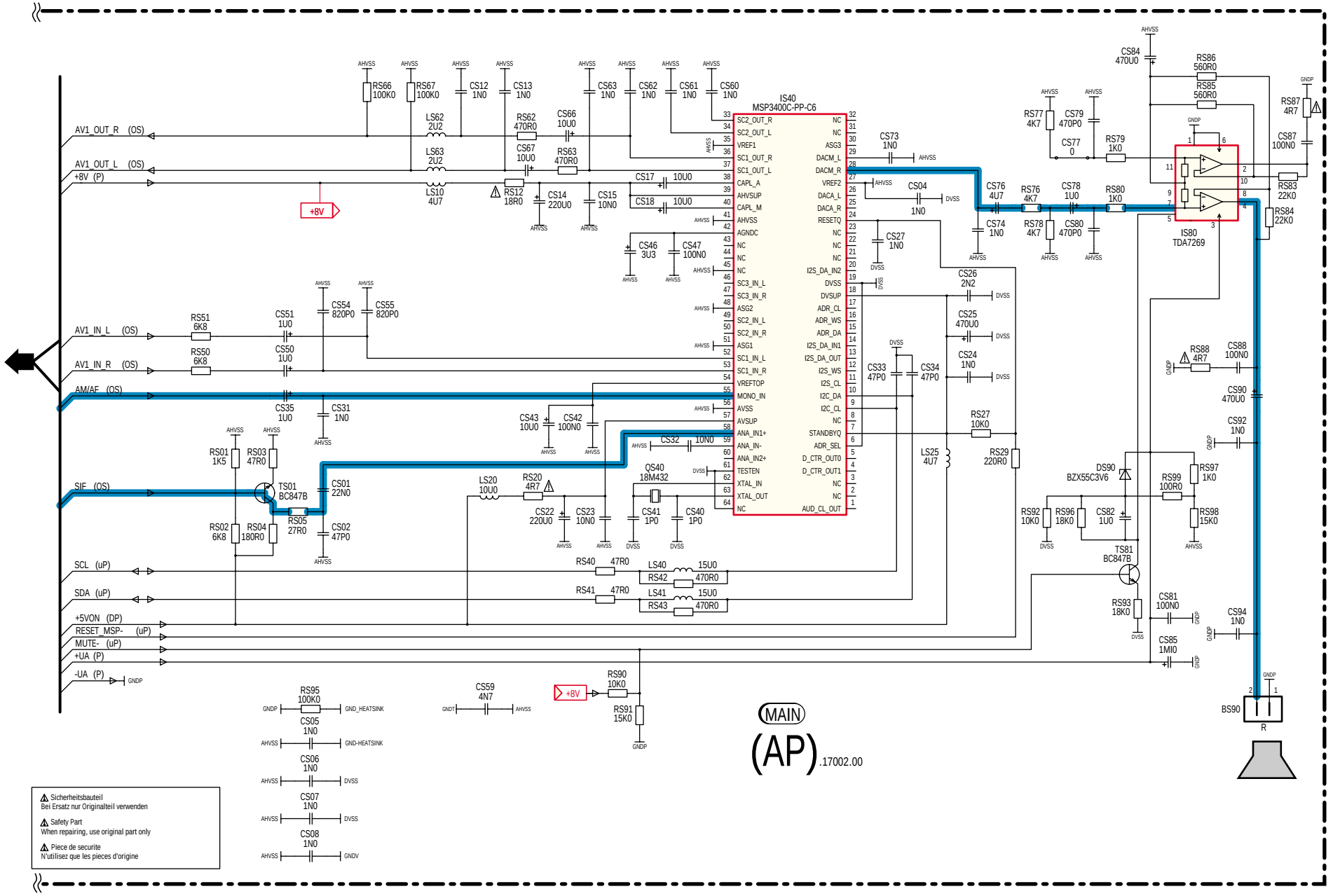
RF/FI/ SCART INTERFACE/VIDEO SIGNAL PROCESSING -HF/FI INTERFACE PERITELEVISION/TRAITEMENT LUMINANCE CHROMINANCE - HF/ZF/ SCART INTERFACE/VIDEO SIGNALVERARBEITUNG - RF/FI /PRESA PERITEL/ELABORAZIONE VIDEO - RF/FI /EUROCONECTOR/TRATAMENTO VIDEO



AMPLIFIER SCHEMATIC DIAGRAM - SCHEMA DE L'AMPLIFICATEUR - SCHALTBILD AUDIO-SIGNALVERABEITUNG - SCHEMA DELL' AMPLIFICATORE
ESQUEMA DEL AMPLIFICADOR
(STEREO)



AMPLIFIER SCHEMATIC DIAGRAM - SCHEMA DE L'AMPLIFICATEUR - SCHALTBILD AUDIO-SIGNALVERABEITUNG - SCHEMA DELL' AMPLIFICATORE - ESQUEMA DEL AMPLIFICADOR
(MONO)



NOTES



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